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Evaluation Of The Silver Tarnish Problem, Launch Processing System

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Space Administration

John F. Kennedy Space Center

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TEST REPORT

Evaluation of The Silver Tarnish Problem, Launch Processing System

ISSUED BY

National Aeronautics and Space Administration
Kennedy Space Center
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ABSTRACT

The Materials Testing Branch was requested to evaluate the effects of silver "tarnishing" of components of the Launch Processing System. The area of most significant concern found is the "tarnish" effects on the wire-wrap wires of the older LPS circuit boards. If maintained in the proper environment the LPS hardware could be expected to have a significantly extended operational life, despite the relatively poor quality of some hardware.

TABLE OF CONTENTS

TABLE OF CONTENTS (CONTINUED)

LIST OF FIGURES

LIST OF FIGURES (CONTINUED)

LIST OF TABLES

1.0 INTRODUCTION

1.1 The Launch Processing System (LPS) was designed in the mid 1970's to provide a ground based computer automated system to control and monitor the Shuttle Transportation System (STS) elements and the associated ground support equipment (GSE), during both the pre-launch processing and the launch countdown. Beginning in 1976 the LPS was installed at the Kennedy Space Center (KSC).

1.2 In the early 1970's silver plating of Integrated circuit (IC) chip leads was a common practice in the electronics industry. However, by the mid-70's the use of silver was being phased out. During the initial purchases of hardware and logistical spares a large quantity of IC's with silver (Ag) plated leads were purchased.

1.3 An additional aspect of the silver (Ag) plating is that a significant number of the LPS IC boards are of the wire-wrap type. The electrical circuits between IC leads (pins) are formed by 30 gauge wire-wrap wires strung between the IC pin socket posts. These 30 gauge wires are silver (Ag) plated copper (Cu) wires.

1.4 The key factor in this evaluation is that the normally accepted operational life of electronics gear is 10 to 15 years. This coupled with the observed "tarnishing" of the silver plated IC pins in the LPS resulted in a request to the Materials Testing Branch (MTB) from the LPS cognizant organizations, NASA, TE-LPS-12, and Grumman Technical Services, GTS-649 to evaluate the silver tarnish

problem. The requestor's were interested in extending the operational life of the LPS an additional 15 years.

2.0 TERMS, DEFINITIONS, AND ABBREVIATIONS

Ag:	Silver
Ag_2S:	Silver Sulfide
Al_2O_3:	Aluminum Oxide
Au:	Gold
Ca:	Calcium
Co:	Cobalt
Cu:	Copper
CuO:	Copper Oxide
DIP:	Dual in-line package, an IC package with two parallel rows of leads (pins).
EDS:	Energy Dispersive Spectroscopy
EDXRF:	Energy Dispersive X-ray Fluorescence
Fe	Iron
HCl	Hydrochloric Acid
H_2S	Hydrogen Sulfide
H_2SO_4:	Sulfuric Acid
IC:	Integrated Circuit, the DIP or the circuits within the package.
LPS:	Launching Processing System
MTBF:	Mean Time Between Failures.
NaCl:	Sodium Chloride
Na_2CO_3:	Sodium Carbonate
$NaHCO_3$:	Sodium Bicarbonate
Na_2S:	Sodium Sulfide
Ni:	Nickel
Pb:	Lead
Pins:	The plated metal leads of an IC DIP.
Post:	Wire-wrap post.
SEM:	Scanning Electron Microscope

Sn: Tin

Socket: The recepticle for an IC pin on a circuit board, including the contacts and the wire-wrap post which extends through the circuit board.

SPC: Shuttle Processing Contract

WDS: Wavelength Dispersive Spectrometry

Wire: 30 gauge, silver plated copper wire used to make wire-wrap circuits.

XPS: X-ray Photoelectron Spectroscope

Zn: Zinc

3.0 SCOPE OF EVALUATION

3.1 REQUESTORS QUESTIONS

The requestor submitted the following list of questions for the Materials Testing Branch to address in the evaluation program.

3.1.1 What is the source of the silver tarnish condition?

3.1.2 Does the tarnish effect the IC DIP's internally?

3.1.3 What is the effect of the tarnish on IC sockets and other components on the board? Is there a problem where the IC pins contact the sockets?

3.1.4 Does the wire-wrap wire show signs of deterioration or brittleness?

3.1.5 What are the near and long term effects on LPS hardware MTBF?

3.1.6 Evaluate protective coatings such as "Contract Re-Nu and Lube."

3.1.7 Is there a suitable method for cleaning the IC pins, wire-wraps, sockets, and other components?

3.2 HARDWARE SUBMITTED

A list of the hardware submitted by the requestors is presented in Table 3-1.

3.3 APPROACH

3.3.1 Initially the following steps were undertaken by the MTB in conducting this evaluation. To expedite the evaluation process these steps were performed as parallel functions and not as serial operations.

3.3.1.1 A literature review was conducted. References to work published by the Materials Science Laboratory (MSL) will be noted by a prefix "M" and will appear in the text as (M1), (M2) etc. External literature will be noted by numbers only as they appear in the list of references.

3.3.1.2 An inspection and analysis of the hardware received was performed to aid in understanding and defining the problem(s). This included visual, microscopic, metalographic, and SEM examination and chemical analysis.

TABLE 3-1
HARDWARE SUBMITTED FOR EVALUATION

ITEM NO.	ITEM	DESCRIPTION
1	WIRE WRAP BOARD 1	MAG. TAPE CONTROLLER BOARD P/N 5551-100334-001 S/N 019250-001
2	WIRE WRAP BOARD 2	HIGH SPEED PARALLEL COMPUTER LINKS P/N 516-200172-001 S/N 54008-002
3	WIRE WRAP BOARD 3	78K00002-70 S/N 004
4	Z80 CPU	MICROCIRCUIT DIGITAL MFG. P/N Z80A CPU/CS DUAL-IN-LINE PACKAGE (DIP)
5	IC (DIP) REPLACED ON BOARD P/N 551-1299-D1-004 S/N 25400-0068	(2) SN74170N, 7545 AND 7627 4-BY-4 REGISTER FILES
6	IC (DIP) REPLACED ON BOARD P/N 551-1338-01-006 S/N 109870-0041	(1) SN74LS170N, 8044 4-BY-4 REGISTER FILE (1) SN74181N, 8018 ARITHMETIC LOGIC UNIT

3.3.1.3 A series of electrical, mechanical and environmental tests and analysis methods were performed on randomly selected elements of the hardware submitted as well as reference components.

3.3.1.4 This project should be considered a survey evaluation utilizing the best engineering judgement available. Some of these areas of interest could warrant a single study unto themselves.

4.0 INSPECTION AND ANALYSIS

Initially the LPS hardware submitted was visually examined, samples removed to determine the materials of construction and the nature of the tarnish, and then a series of microscopic, metallographic, and SEM examination were performed.

4.1 IC BOARD NO. 1

4.1.1 Board No. 1, Magnetic Tape Controller Board, was visually examined (see Figure 4-1 and 4-2). The board contained approximately 280 black body IC sockets with wire-wrap posts. The majority of the sockets contained IC's which carried date codes ranging from 1971 through 1975.

4.1.2 The pin leads on many of the IC's were tarnished (see Figure 4-3). The exposed wire-wrap wires were found to have varying shades of discoloration (tarnish) on the exposed wire (see Figure 4-4). There was

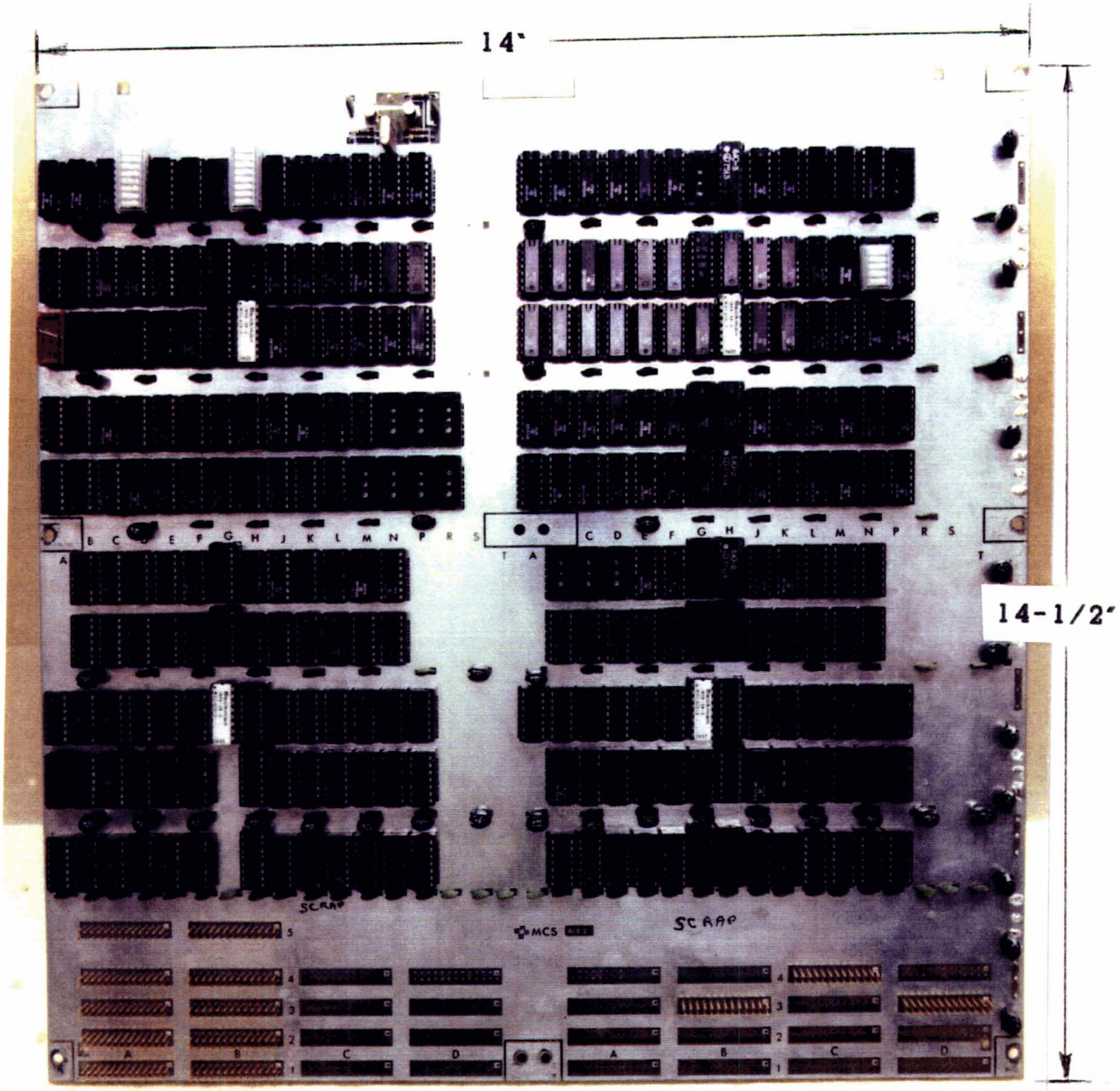


FIGURE 4-1

THE TOP (IC) SIDE OF BOARD NO. 1, MAGNETIC TAPE CONTROLLER, IS SHOWN.

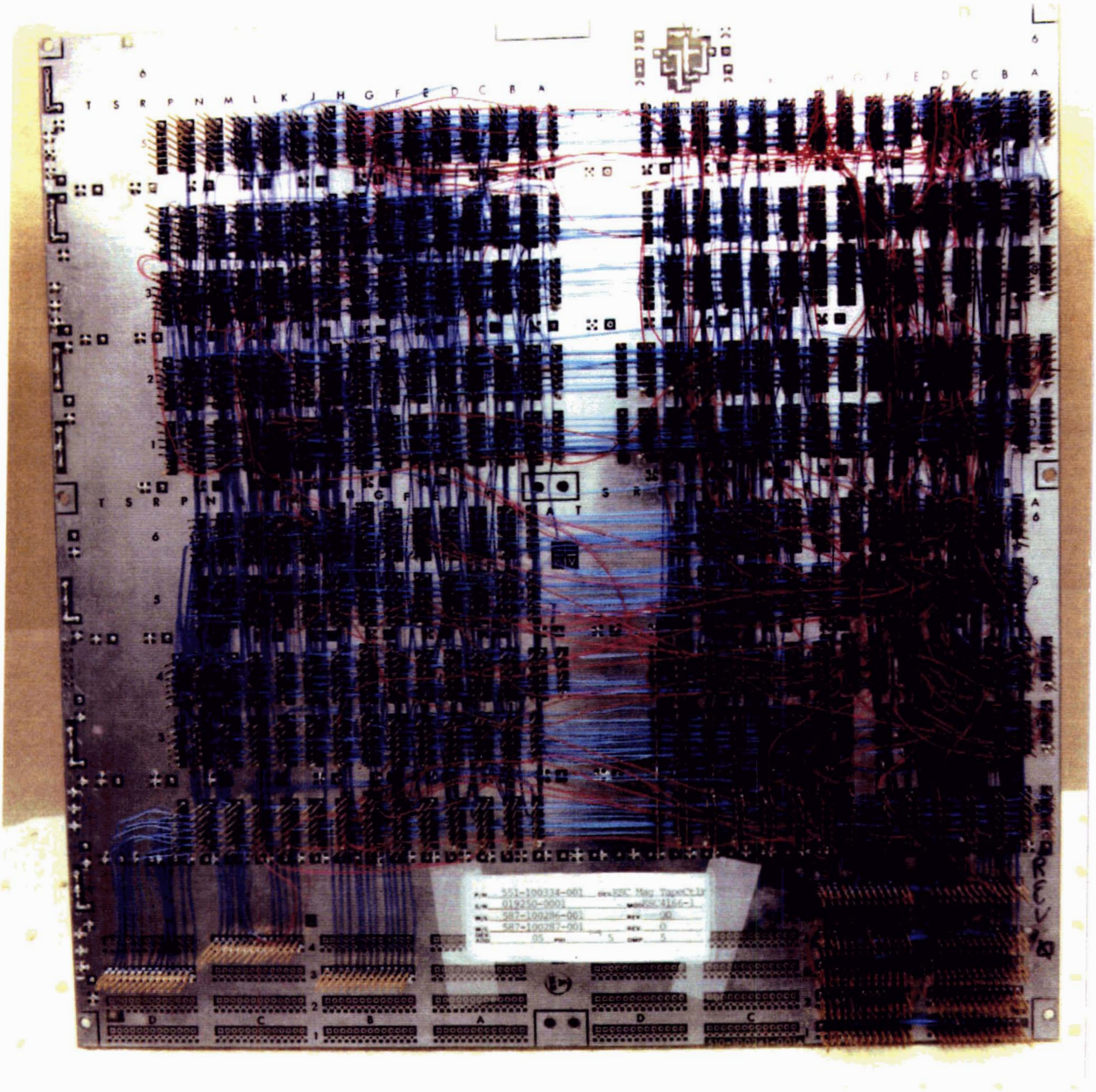


FIGURE 4-2

THE BOTTOM (WIRE-WRAP) SIDE OF BOARD NO. 1, MAGNETIC TAPE CONTROLLER, IS SHOWN.

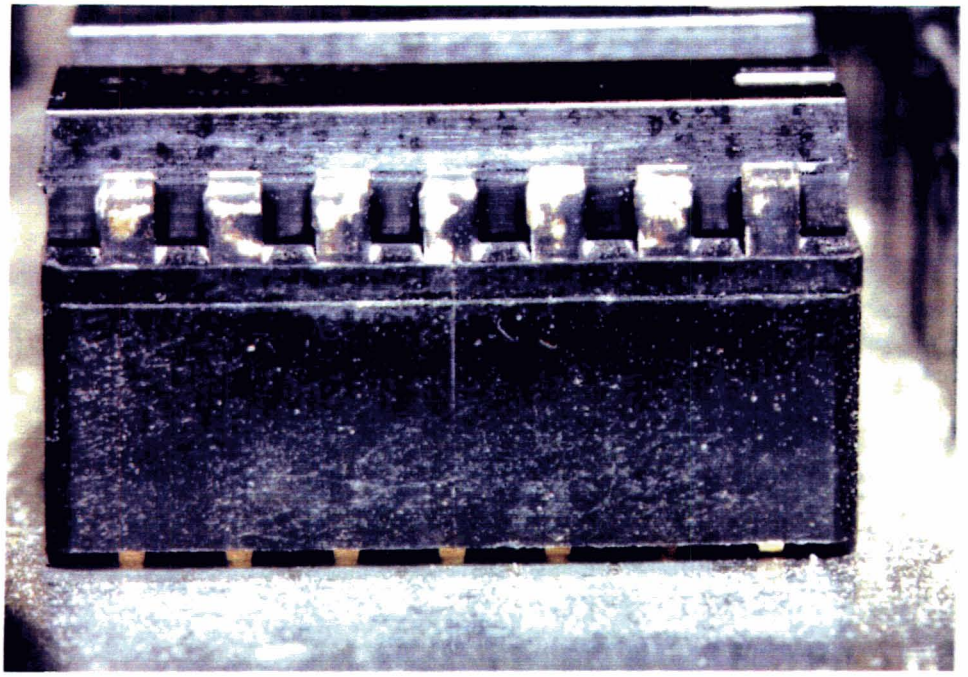


FIGURE 4-3

AN IC WITH TARNISHED (BLACKENED) SILVER LEADS (PINS) ON BOARD NO. 1 IS SHOWN. ENVIRONMENTAL DEBRIS IS EVIDENT ON THE BOARD AND THE SIDE OF THE BLACK BODY SOCKET.

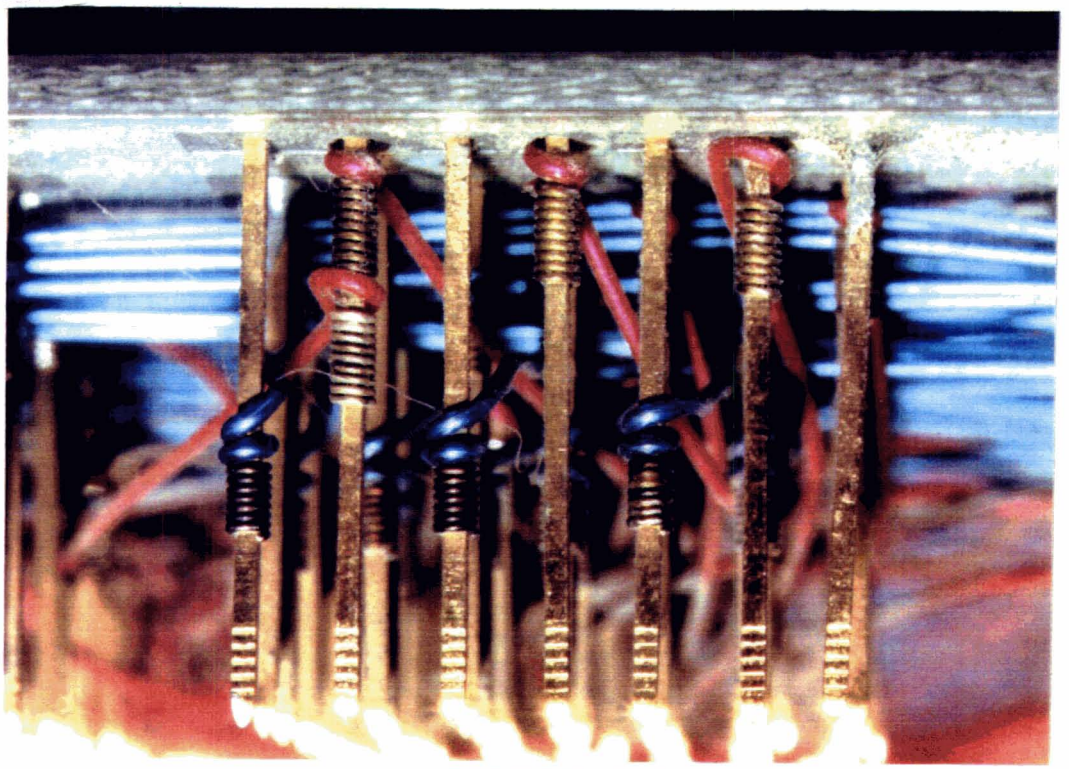


FIGURE 4-4

WIRE-WRAPS ON BOARD NO. 1 ARE SHOWN. THE EXPOSED WIRES RANGED IN COLOR FROM SILVER THROUGH GOLDEN TO BLACK. ENVIRONMENTAL DEBRIS IS EVIDENT ON SEVERAL POSTS WHERE THEY PENETRATE THE BOARD.

some environmental debris on the surfaces of the Board. The pin and wire tarnish was predominantly near one edge of the board. The long wire-wrap wire runs were laid-in geometrically close to the board and held down by the overlapping short wire runs.

4.1.3 Microchemical analysis of material samples on Board No. 1 indicated the following:

a. IC pin materials primarily Fe-Co-Ni or Fe-Ni alloys with Ag plating. There were a few IC's with Sn plated Fe (low alloy steel) pins.
b. The sockets were Cu with Au plating.
c. The wire-wrap wire was Cu with Ag plating.
d. The tarnish was found to be Ag_2S.

4.2 IC BOARD NO. 2

4.2.1 Board No. 2, high speed parallel computer link, was visually examined, it was similar to Board No. 1 (but half the size). The board contained approximately 125 black body IC sockets with wire-wrap posts. The majority of the sockets contained IC's which carried date codes or 1979 and 1981.

4.2.2 The majority of IC pins were bright and shiny (see Figure 4-5) and the wire-wrap wires were also a bright silver in color (see Figure 4-6). Many of long wire-wrap wires appeared to be hanging loose like random strands of cooked spaghetti.

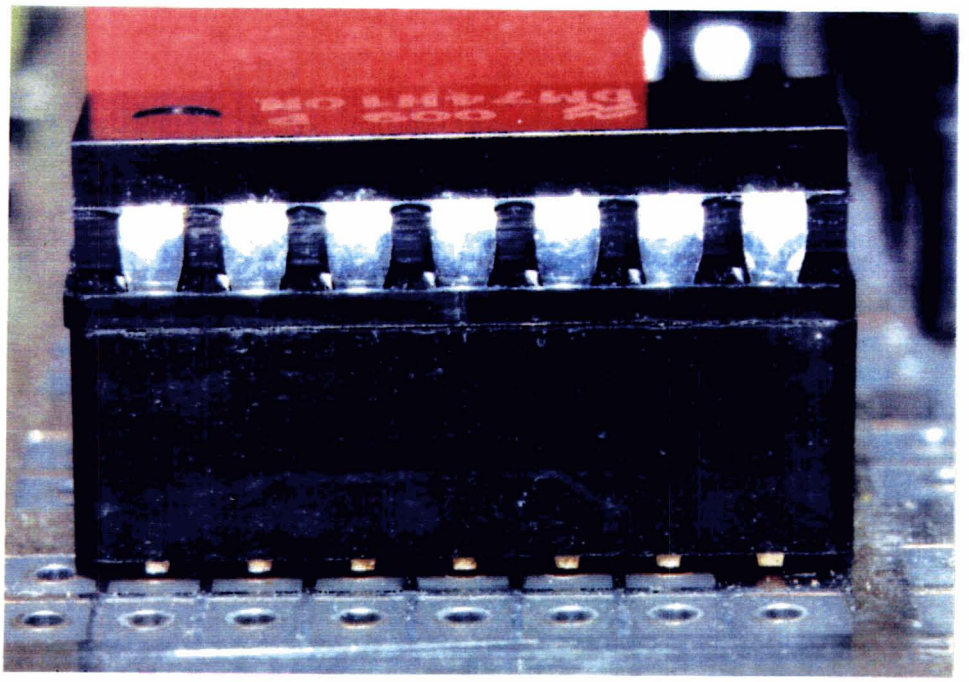


FIGURE 4-5

AN IC WITH TYPICAL SHINY PINS ON BOARD NO. 2 IS SHOWN.

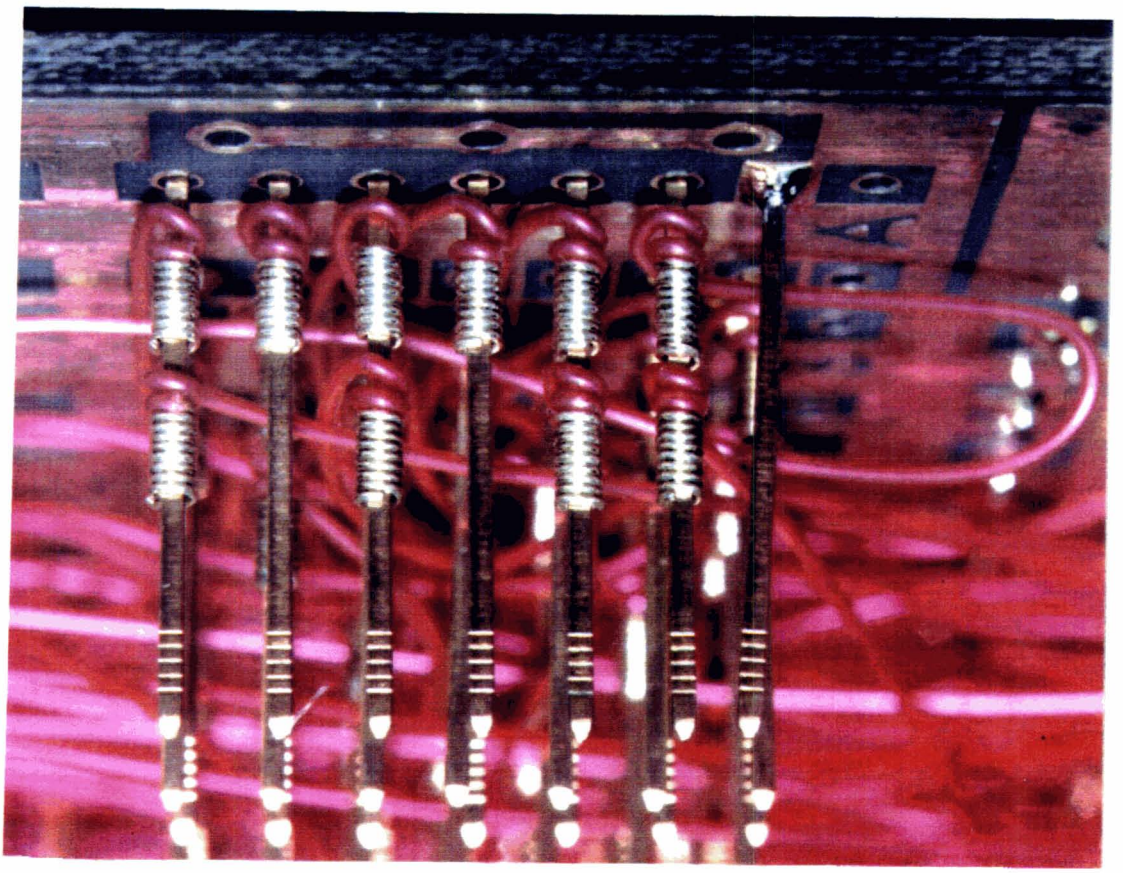


FIGURE 4-6

WIRE-WRAPS ON BOARD NO. 2 ARE SHOWN. THE EXPOSED WIRES WERE ALL BRIGHT AND SHINY SILVER IN COLOR.

4.2.3 Microchemical analysis of material samples from Board No. 2 indicated the following:

a. IC pin materials are Cu or Ni-steel with Sn plating.
b. The sockets are Cu-Ni alloy. The wire-wrap post portion is unplated, and the socket pin clip portion is Au plated.
c. The wire-wrap wire was Cu with Ag plating.

4.3 IC BOARD NO. 3

4.3.1 Board No. 3, designation unknown, was visually examined. The board was fabricated as a socket panel, the individual pin sockets with wire-wrap posts were installed as integral parts of the board (see Figure 4-7). The board contained socket sets to accommodate approximately 189 IC's of the 16-pin DIP configuration. Approximately 145 IC's were installed which carried data codes ranging from 1974 through 1976.

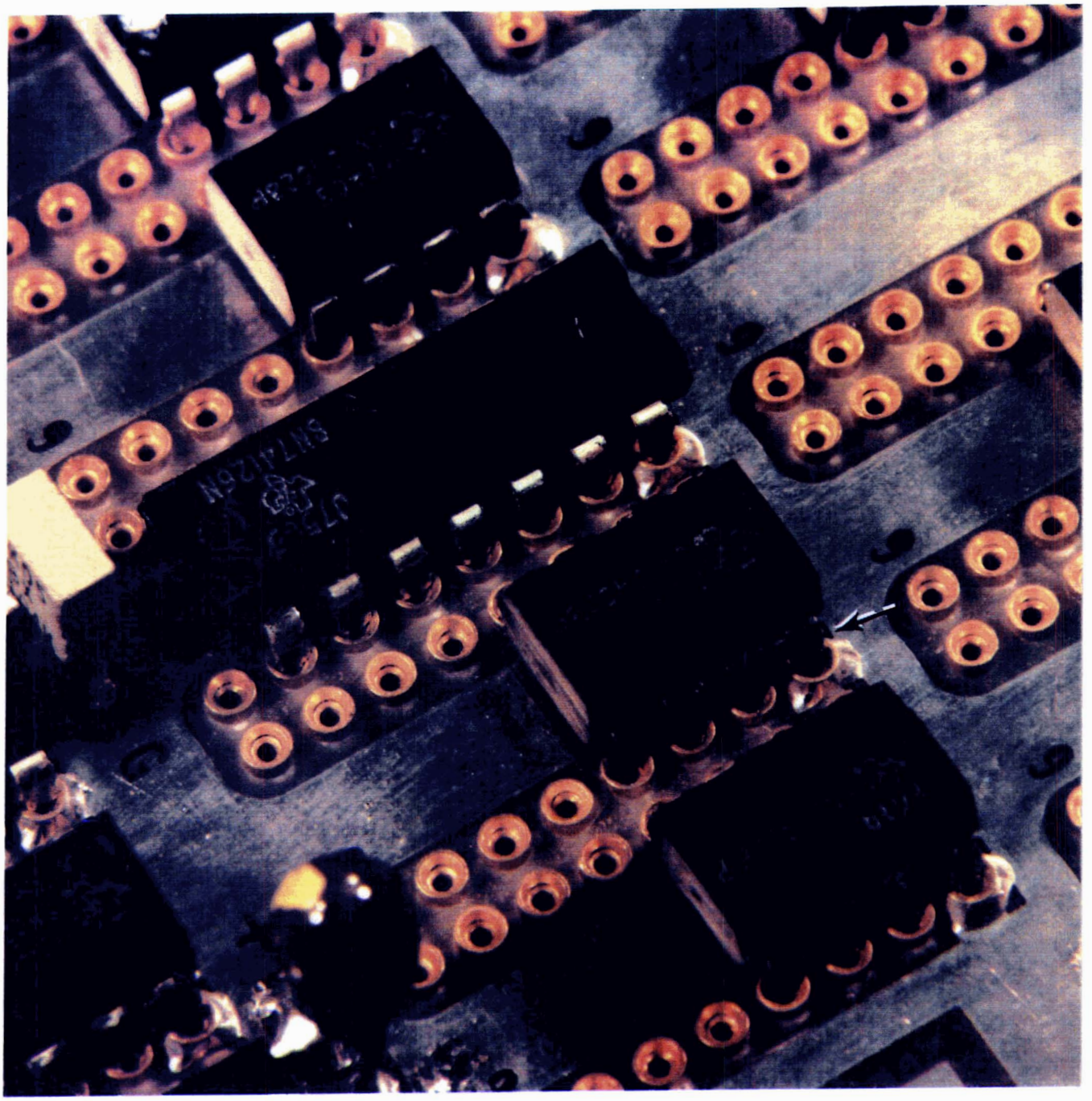


FIGURE 4-7

THE SOCKET/POSTS ARE AN INTEGRAL PART OF BOARD NO. 3. THE SILVER PLATED IC PINS (ARROW) ARE BLACK FROM AN INADVERTENT EXPOSURE TO H_2S.

4.3.2 Initially only a few IC pins and wire-wrap wires near one edge of the board were tarnished. However, the entire board was inadvertently exposed to H_2S vapors in the laboratory which tarnished most of the exposed Ag. The long wire-wrap wire runs were laid out geometrically and like Board No. 1 were held down by overlapping short wire runs.

4.3.3 Microchemical analysis of the material samples from the Board No. 3 identified the following:

a. The pins of the 1976 IC's were Fe-Ni alloys plated with both Ag and Pb-Sn.
b. The sockets were Cu with Au plating.
c. The wire was Cu with Ag plating.

4.4 SUMMARY OF BOARD EXAMINATION

The primary IC pin, socket, and wire material information is presented in Table 4-1.

4.4.1 Board No. 1 was found to be the most aged or weathered board of the three. When received it had a significant amount of environmental debris clinging to the board, the most evidence of tarnished IC pins, and it contained IC's with date code of 1975 or earlier. It is estimated that Board No. 1 is original LPS hardware dating back to the 1975 to 1976 time frame. The board is probably 12 years old.

TABLE 4-1
MATERIALS OF CONSTRUCTION LPS IC BOARDS

BOARD NUMBER	MATERIALS						IC		EST. BOARD MFG. DATE
	WIRE		SOCKET		IC PINS		DATE CODE	PART NUMBER	
	BASE	PLATING	BASE	PLATING	BASE	PLATING			
1	Cu	Ag	Cu	Au	Fe	Sn	7432	8198-38-0	
					Fe-Co-Ni	Ag	7349	SN7495AN	
					Fe-Ni	Ag	7148	SN74451N	1974/76
2	Cu	Ag	Cu Ni	Au None on Post	Cu	Sn	7949	SN74H04N	
					Fe-Ni	Sn	8122	SN54LS170N	1981/82
3	Cu	Ag	Cu	Au	--	Pb/Sn	7615	SN74157AN	
					Fe-Ni	Ag	7405	SN75452BP	
					Fe-Ni	Ag	615	SN75752BP	1976/78

4.4.2 Board No. 2 was found to be free of tarnish and didn't appear to be weathered. The date codes on the IC's were predominantly 1979 through 1981 vintage. The board is probably 6 years old.

4.4.3 Board No. 3 when received showed little evidence of aging or weathering. There was some light tarnishing of some IC pins and exposed wire-wrap wire. The date codes on the IC's were predominantly 1974 through 1976. THe board may be 10 to 12 years old.

4.5 IC's REMOVED FROM STOCK

Two Z80 CPU IC's were removed from stock by the requestors. The pins were found to be tarnished. The discoloration encompassed a rainbow spectrum of colors including black (see Figure 4-8).

4.5.1 The IC's had been supplied in military standard type packages (see Figure 4-9). The packaging markings, "3/84" indicated that the IC's were packaged in 1983.

4.5.2 Examination of IC's (see Figure 4-10) indicated that the IC DIP's were manufactured during the 26th week of 1981 in the Philippines.

4.5.3 SEM/EDS analysis indicated that the base metal of the IC pins to be a high-Ni steel with a trace of Mn. SEM/EDS analysis showed the plating to be Ag with S present. The discoloration is probably Ag_2S, tarnish.

FIGURE 4-8

THE DISCOLORED PINS OF A Z80 CPU IC ARE SHOWN.

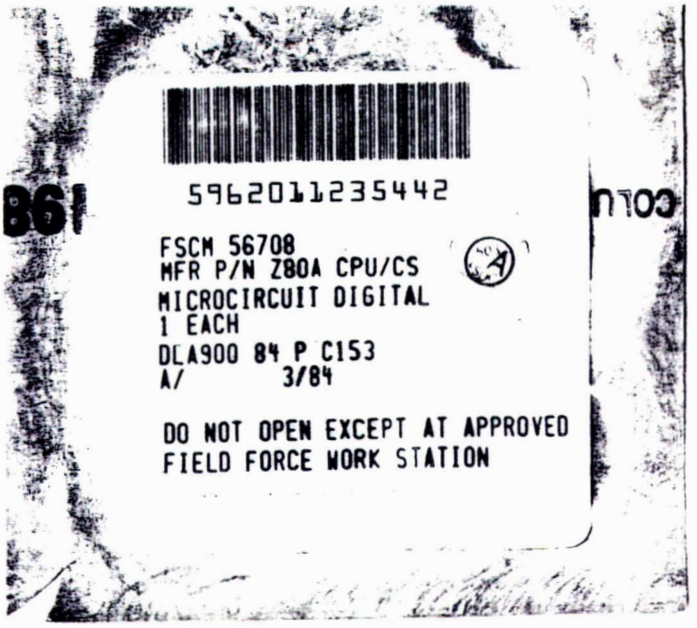


FIGURE 4-9

THE Z80 PACKAGING, MIL-B-117E, WAS DATED 3/84

FIGURE 4-10

ONE OF THE Z80 IC's IS SHOWN. THE MARKINGS INDICATE THAT THE IC WAS MANUFACTURED DURING THE 26th WEEK OF 1981, IN THE PHILIPPINES.

4.5.4 The IC's may have become tarnished in the period between manufacture in 1981 and packaging in 1984.

4.6 IC'S REMOVED DURING LPS BOARD REPAIR

The two pairs of IC's removed from LPS circuit boards during troubleshooting operations were examined and found to have tarnished pins similar to those previously noted in Figures 4-3 and 4-8 (Reference Table 3-1 items 5 and 6 for a description of these IC's).

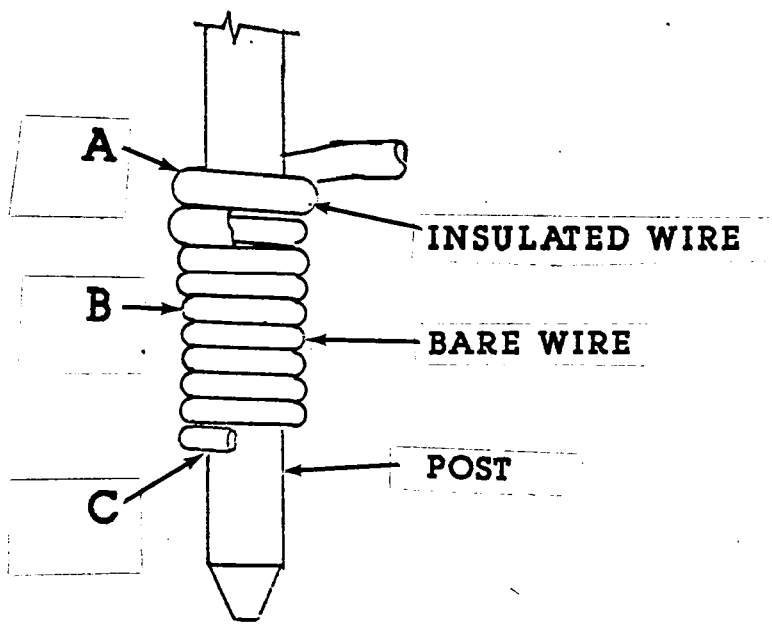


FIGURE 4-11

THE AREAS OF THE WIRE-WRAP WIRES EXAMINED METALLOGRAPHICALLY ARE IDENTIFIED.

4.7 WIRE-WRAP WIRE

Several heavily tarnished wire-wrap wires from Board No. 1 were examined metallographically. The locations of the areas examined are listed below and illustrated in Figure 4-11 on previous page:

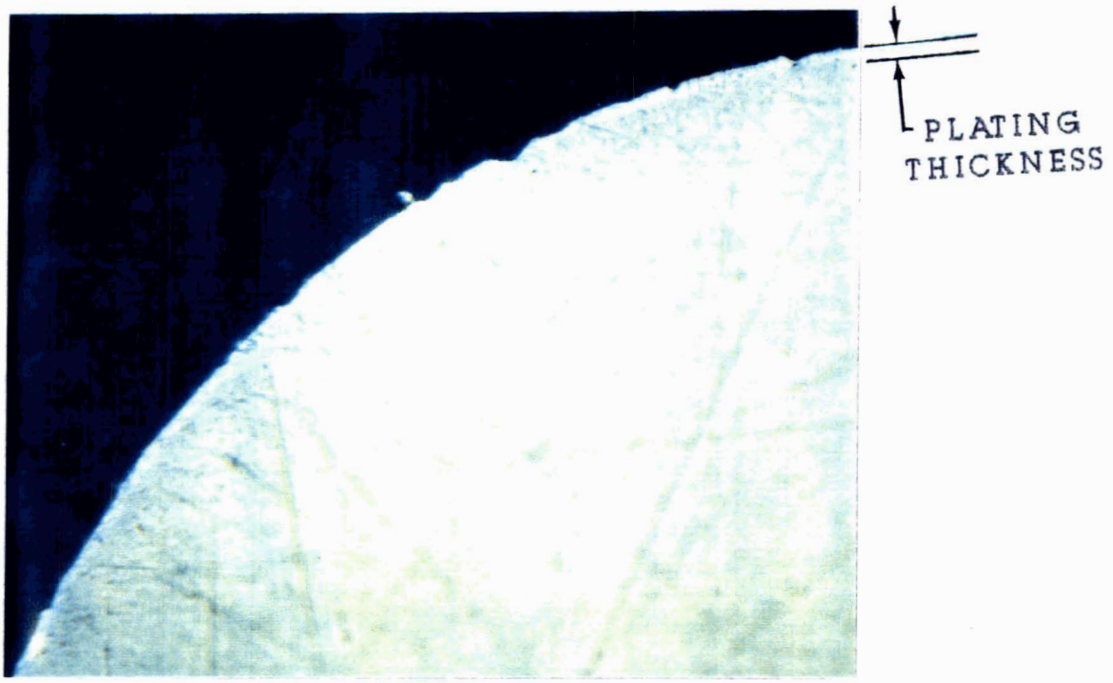
A. Wire under insulation.
B. Bare wire in the middle of the wrap.
C. Bare wire near the wire end.

4.7.1 The silver plating was found to be approximately 40 to 60 microinches or 10,000 to 15,000 angstroms thick (see Figure 4-12).

4.7.2 The majority of the wire protected by the insulation in area "A" was uneffected by the H_2S environment (see Figure 4-12). One of the 7 area "A" specimens showed evidence of corrosion penetrating the protective silver plating (see Figure 4-13).

4.7.3 The exposed wires in area "B" showed some evidence of corrosion penetration into the Cu (see Figure 4-14).

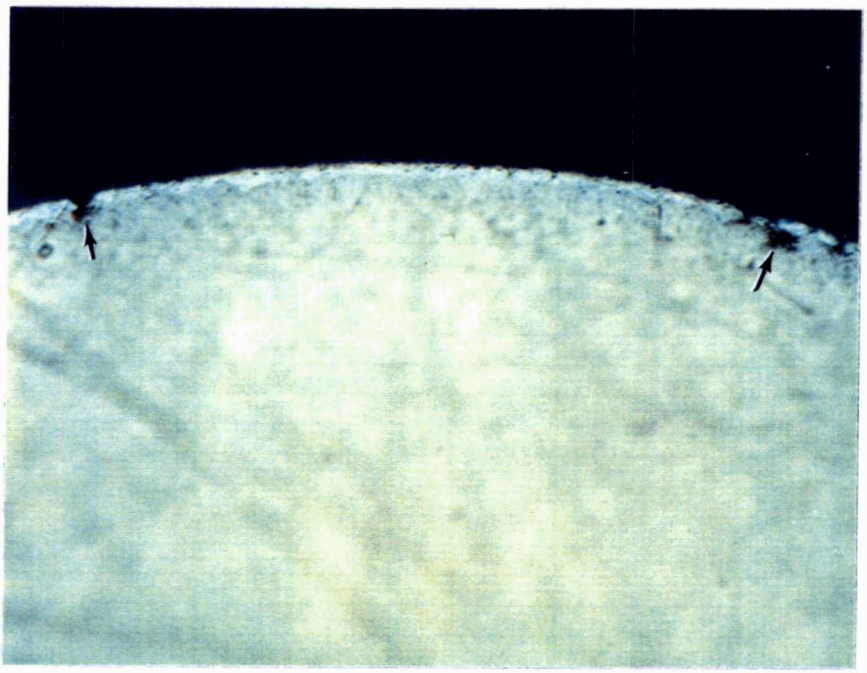
4.7.4 The exposed wire close to the ends which are probably subjected to the most stress and damage during the wire-wrap process, showed the greatest evidence of corrosive attack (see Figure 4-15).



MAGNIFICATION: 1000X

FIGURE 4-12

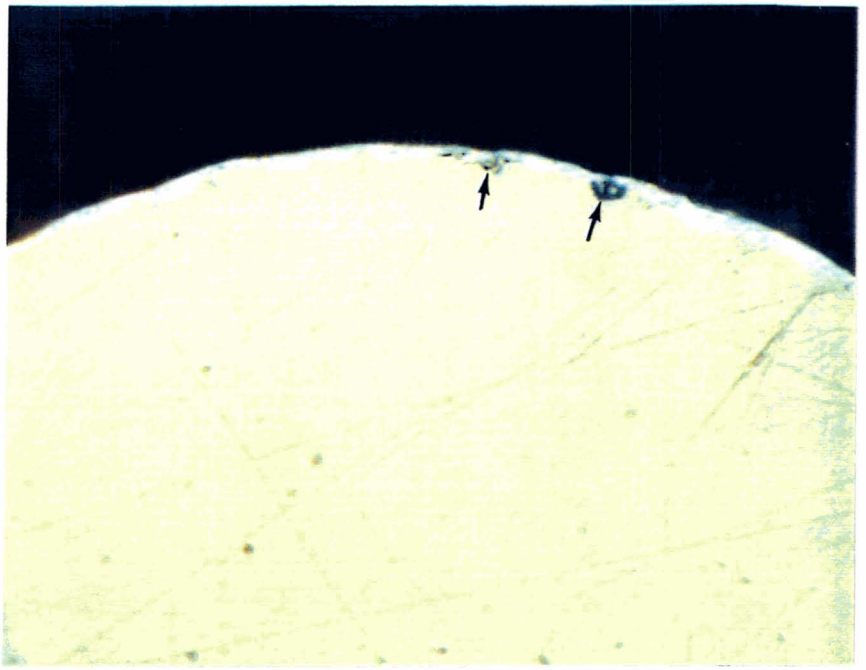
PHOTOMICROGRAPH OF A TYPICAL AREA 'A' WIRE CROSS-SECTION. THE Ag PLATING HAS BEEN SUBJECTED TO MECHANICAL DAMAGE ONLY.



MAGNIFICATION: 1000X

FIGURE 4-13

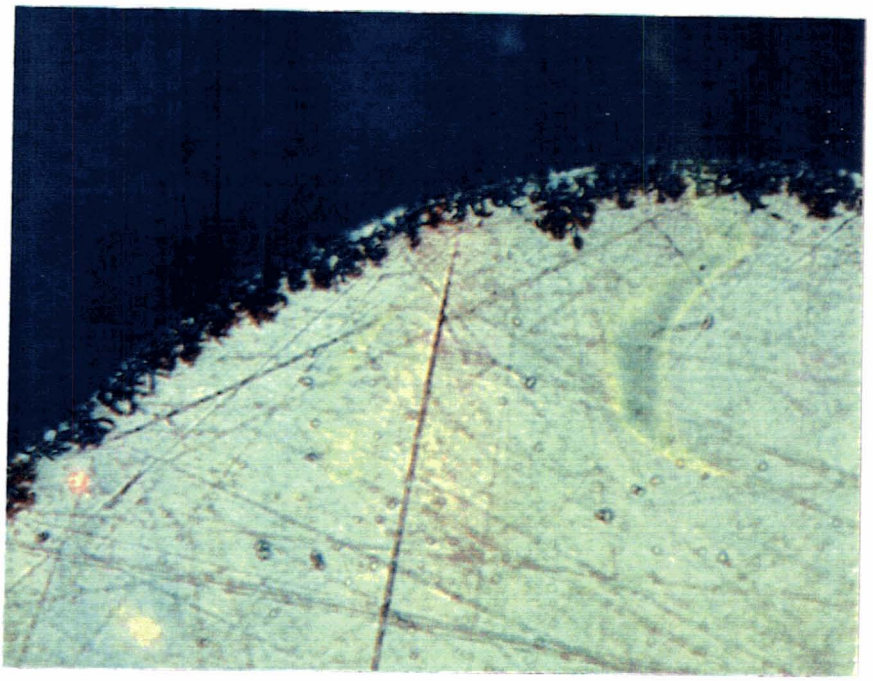
PHOTOMICROGRAPH OF THE SINGLE AREA 'A' WIRE CROSS-SECTION WHICH SHOWED SIGNS OF CORROSION PENETRATING THE Ag PLATING.



MAGNIFICATION: 1000X

FIGURE 4-14

PHOTOMICROGRAPH OF A TYPICAL AREA 'B' WIRE CROSS-SECTION WHICH SHOWS SIGNS OF CORROSION PENETRATING IN TO THE Cu.



MAGNIFICATION: 1000X

FIGURE 4-15

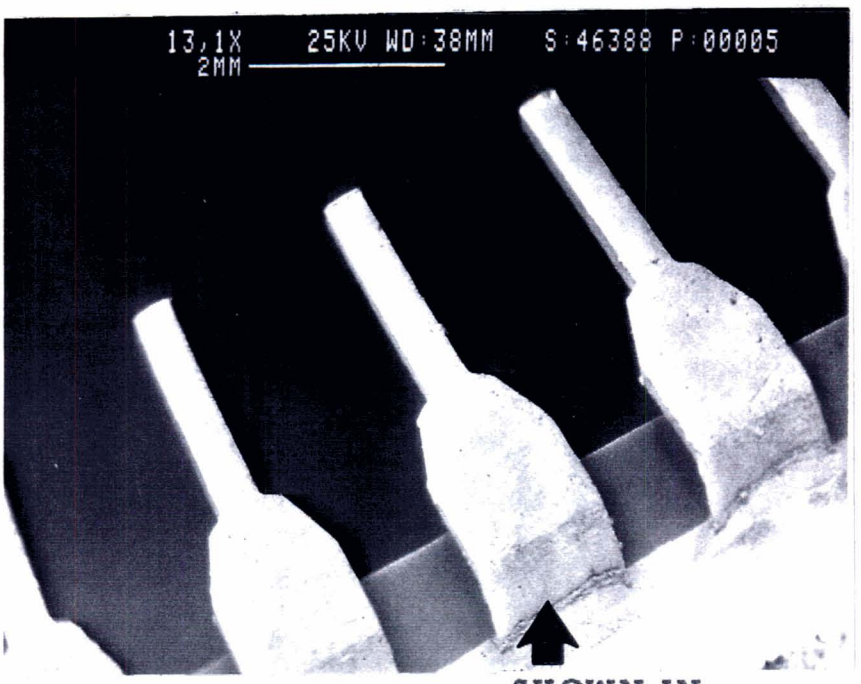
PHOTOMICROGRAPH OF AN AREA 'C' WIRE CROSS-SECTION WHICH SHOWS GROSS CORROSION PENETRATION INTO THE Cu.

4.8 IC PINS

The pins of IC's from all three boards and other sources were microscopically examined. From these, several IC's were selected for SEM/EDS analysis and documentation to illustrate the variations between the pins of different IC's.

4.8.1 The pins of an IC from Board No. 2 were examined. The pins from the model number SN54LS170J IC, with a date code of 8122A were a Ni-steel, with a Sn coating (plating). The coating was found to contain only a few minute voids or pits; however, there was some surface roughness in the bend area (see Figure 4-16). The contact area (see Figure 4-17) shows signs of sliding contact, scratches, while some of the adjacent areas show sign of florescence. Florescence in SEM analysis is often a sign of oxidation, corrosion. The contact area face of the pins is relatively flat and perpendicular to the adjacent planes, and it extends the full thickness of the pin.

4.8.2 The pins of an IC which was obtained new from a commercial hobby source were examined. The IC's model number was SN7404N, with a date code of 748C. The pins were Cr-steel, with a Pb-Sn coating. The coating was found to contain a few voids or pits (see Figures 4-18 and 4-19) and the coating appeared to be relatively thicker than that on the pins of the previous IC, SN54L5170J. One of the voids was noted to have a high Si content. This IC was unused.



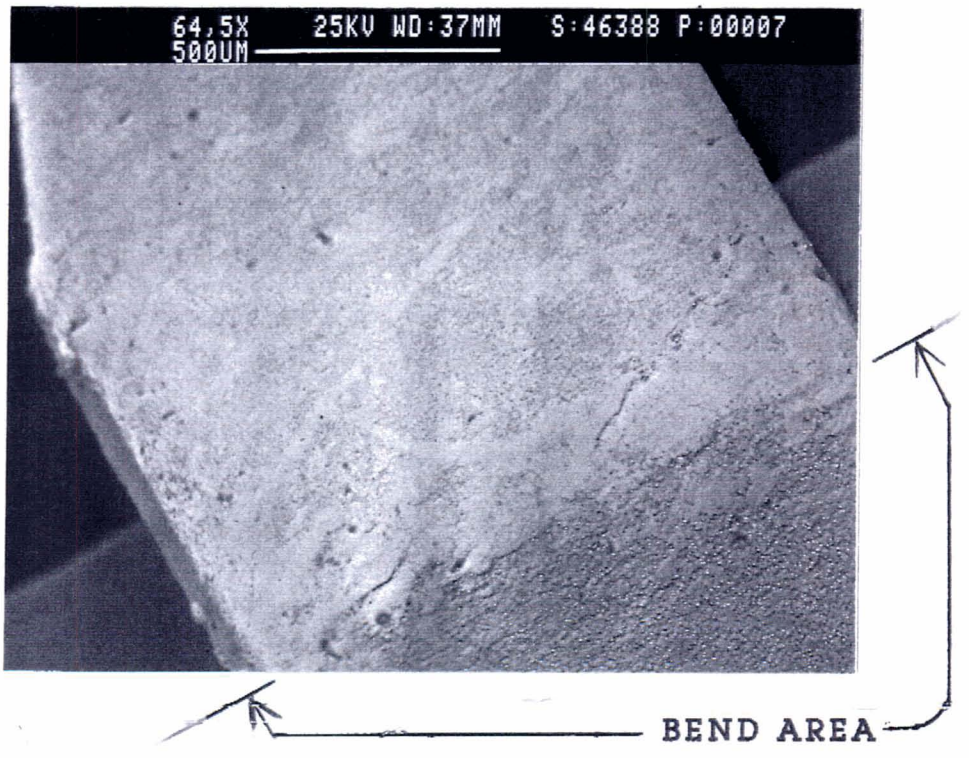


FIGURE 4-16

SEM-PHOTOMICROGRAPHS OF THE Sn PLATED PINS OF IC SN54LS170J, 8122, BOARD NO. 2. SURFACE ROUGHNESS IS EVIDENT IN THE BEND AREA (LOWER VIEW).

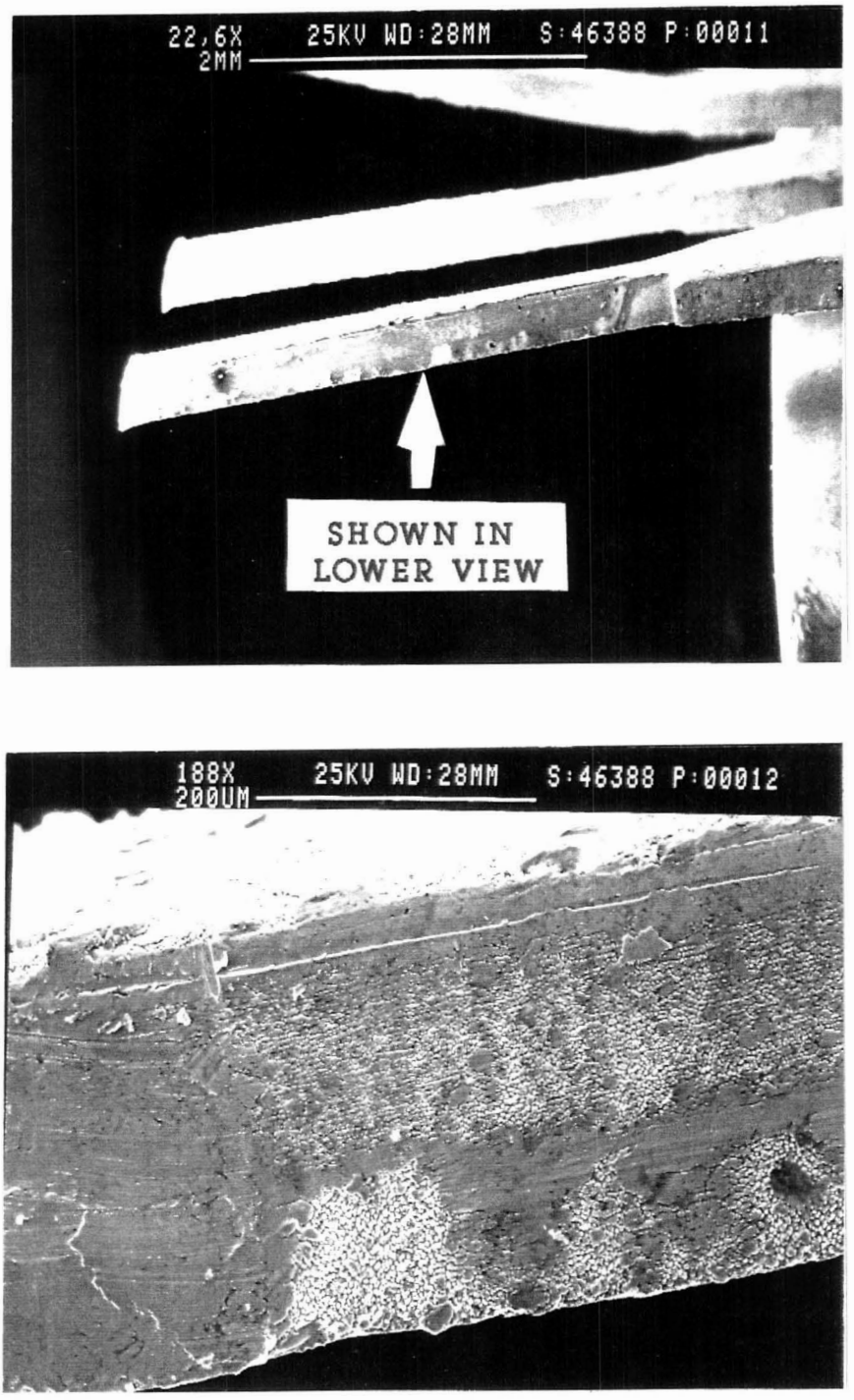


FIGURE 4-17

SEM-PHOTOMICROGRAPHS OF A Sn PLATED PIN CONTACT AREA (ARROW) OF IC SN54LS170J, 8122, BOARD NO. 2. THE CONTACT AREA IS A FLAT SURFACE WHICH TRAVERSES THE THICKNESS OF THE PIN. SOME SCRATCHES ARE EVIDENT FROM INSTALLATION IN AND REMOVAL FROM THE SOCKET.

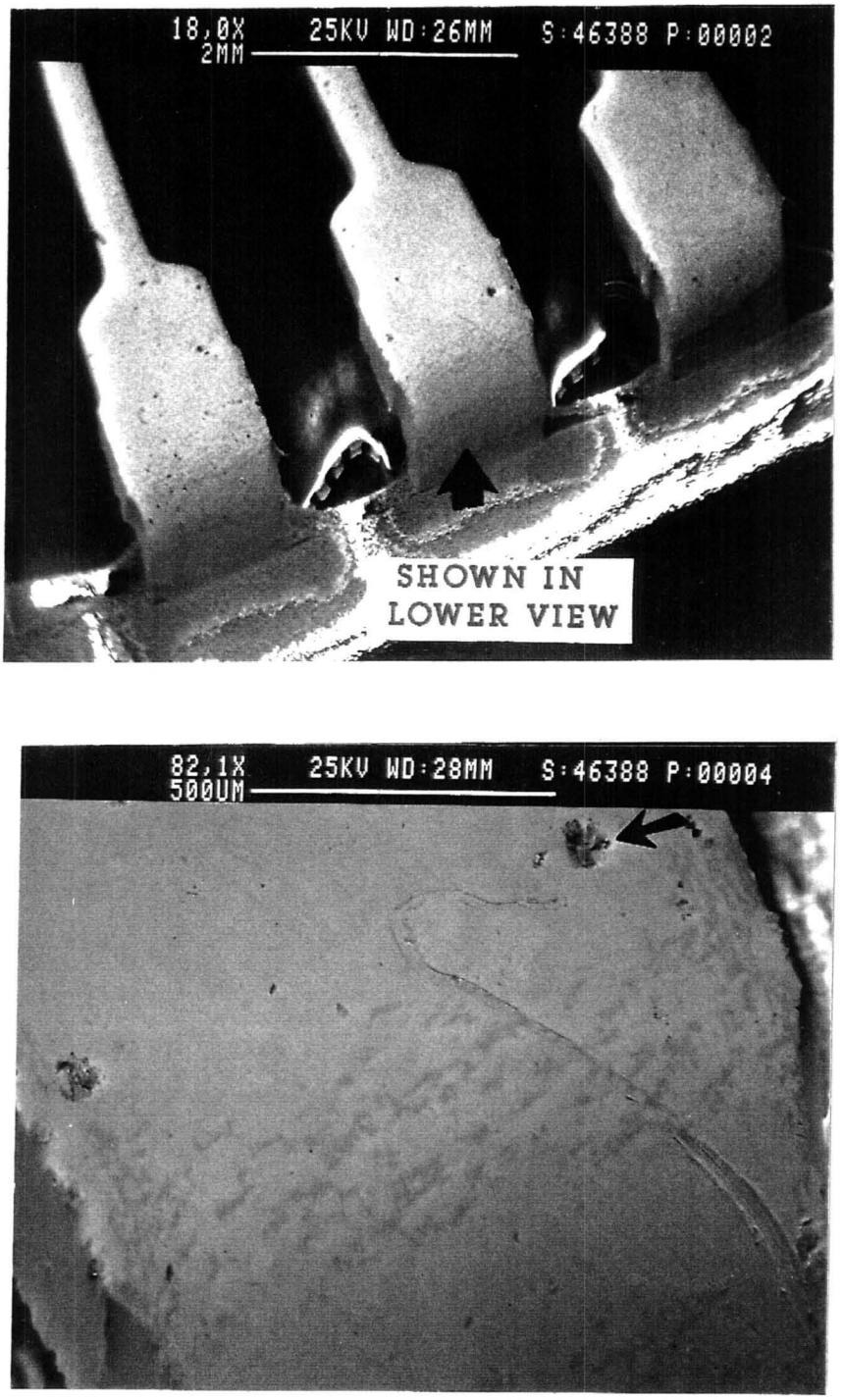


FIGURE 4-18

SEM-PHOTOMICROGRAPHS OF THE Pb-Sn PLATED PINS OF IC SN7404N, (8)748. THE PIT (ARROW) CONTAINED Si.

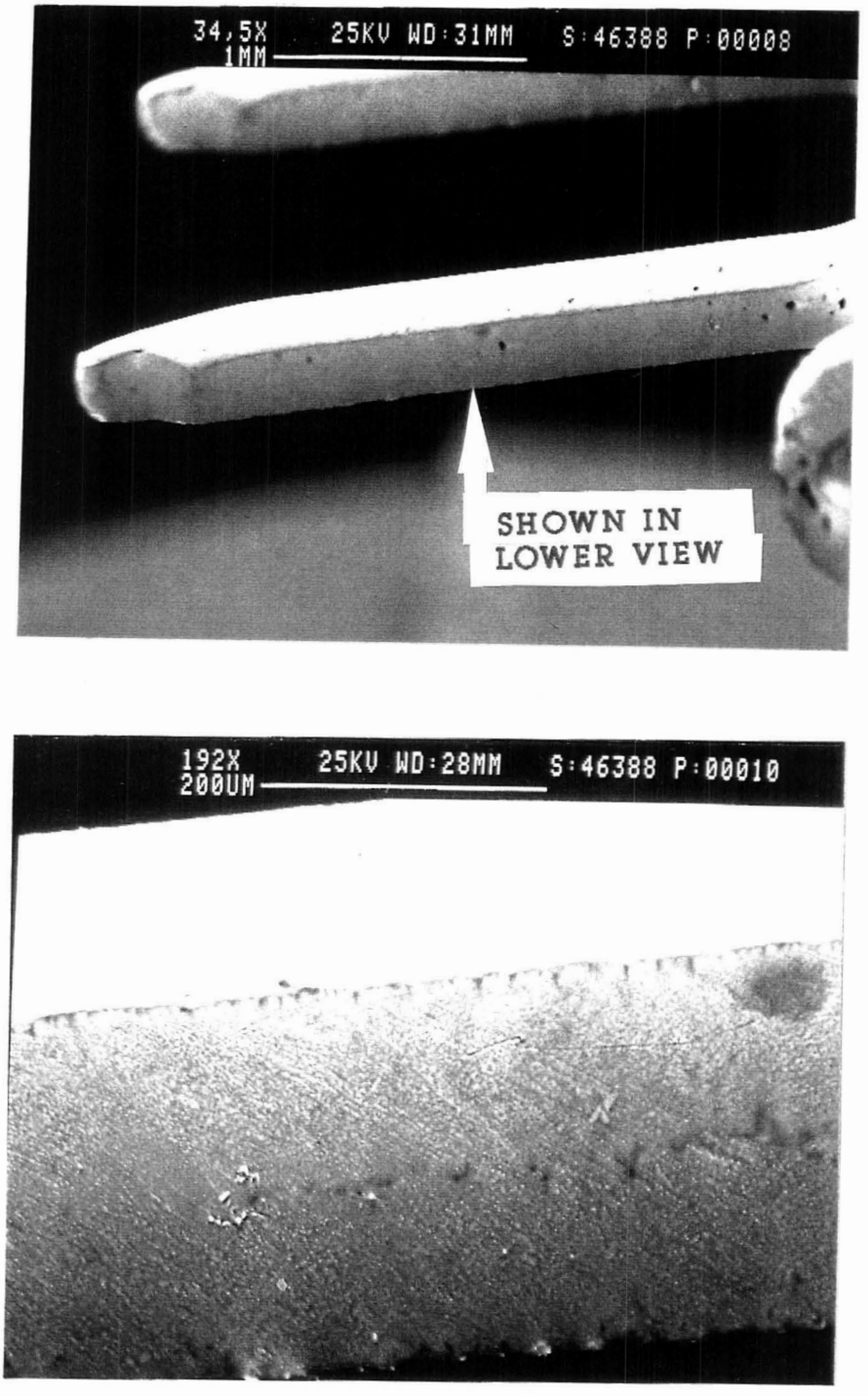
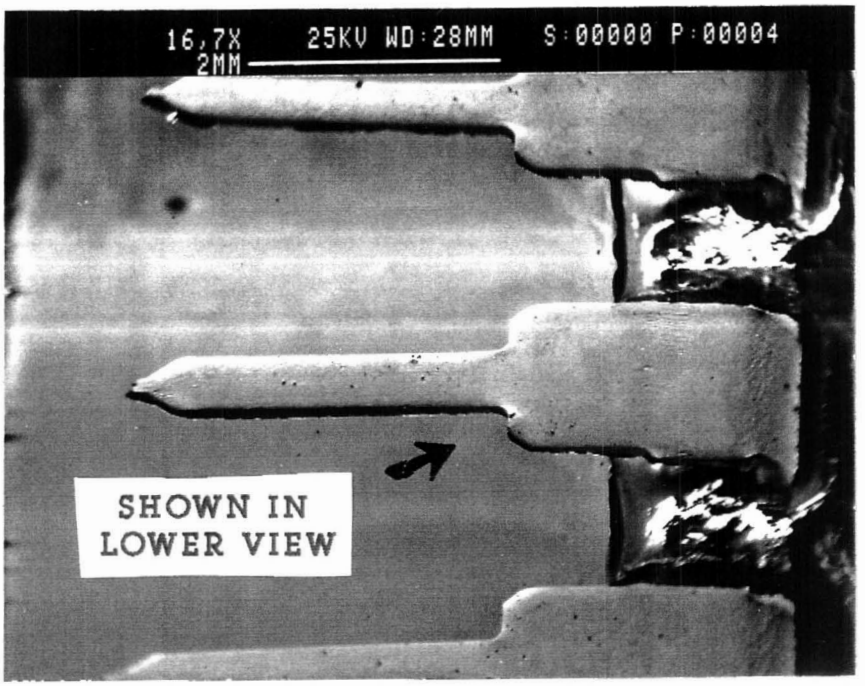


FIGURE 4-19

SEM-PHOTOMICROGRAPHS OF A Pb-Sn PLATED PIN OF IC SN7404N, (8)748. THIS IC WAS UNUSED.

4.8.3 The pins of an IC randomly selected from Board No. 1 was examined. The IC's model number was not documented. The pins appeared to have a relatively heavy coating of Ag over the Fe-Co-Ni alloy (see Figure 4-20). On approximately half of the depth of the contact face (see Figure 4-21) the surface appears rough beneath the Ag coating. Smearing of the Ag coating due to contact with the socket is evident. The actual contact area traversed less than half of the pin thickness.

4.8.4 A second IC from Board No. 1, Model SN7495AN, BS7349, was selected for SEM/EDS analysis and documentation. The pins were a Ni-steel with Ag plating. There were numerous black areas and spots on the pins (see Figure 4-22). The areas of black have a high Si content. It was noted that the S content was much less than on other Ag plated IC pins previously analyzed. In the bend area an "orange peel" or "mud cracking" was evident through the thin Ag plating (see Figure 4-22). This is considered typical of stress corrosion. The contact area surfaces (see Figure 4-23) showed a distinct variation across the surface. This may be associated with the stamping process which formed the pins and/or the plating process. This variation appears to reduce the pin/socket contact area in the case of the black body sockets. Si and Cl were found in the pin contact areas.



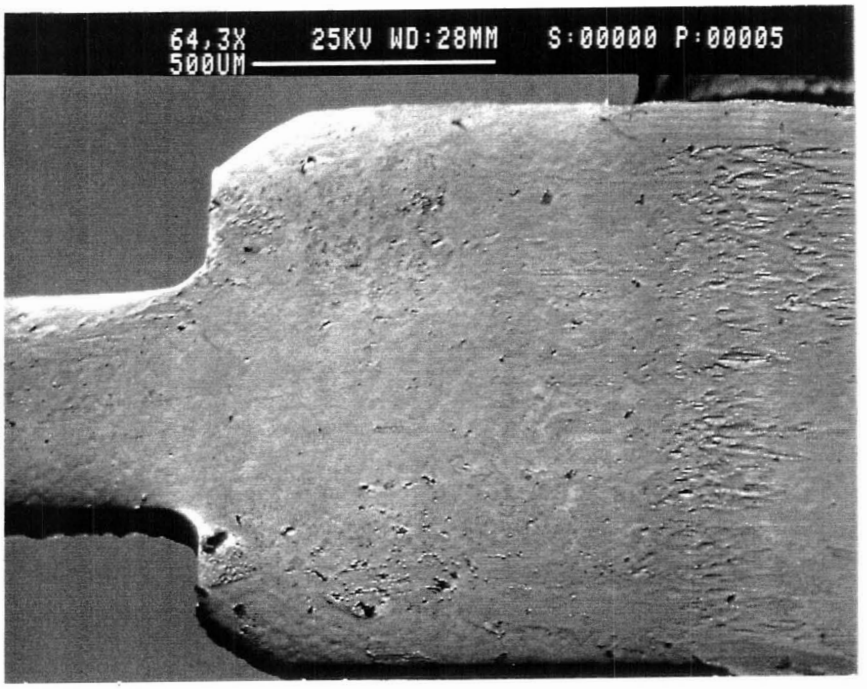


FIGURE 4-20

SEM-PHOTOMICROGRAPHS OF THE Ag PLATED PINS OF AN IC FROM BOARD NO. 1. THE Ag COATING APPEARS TO BE RELATIVELY HEAVY/THICK.

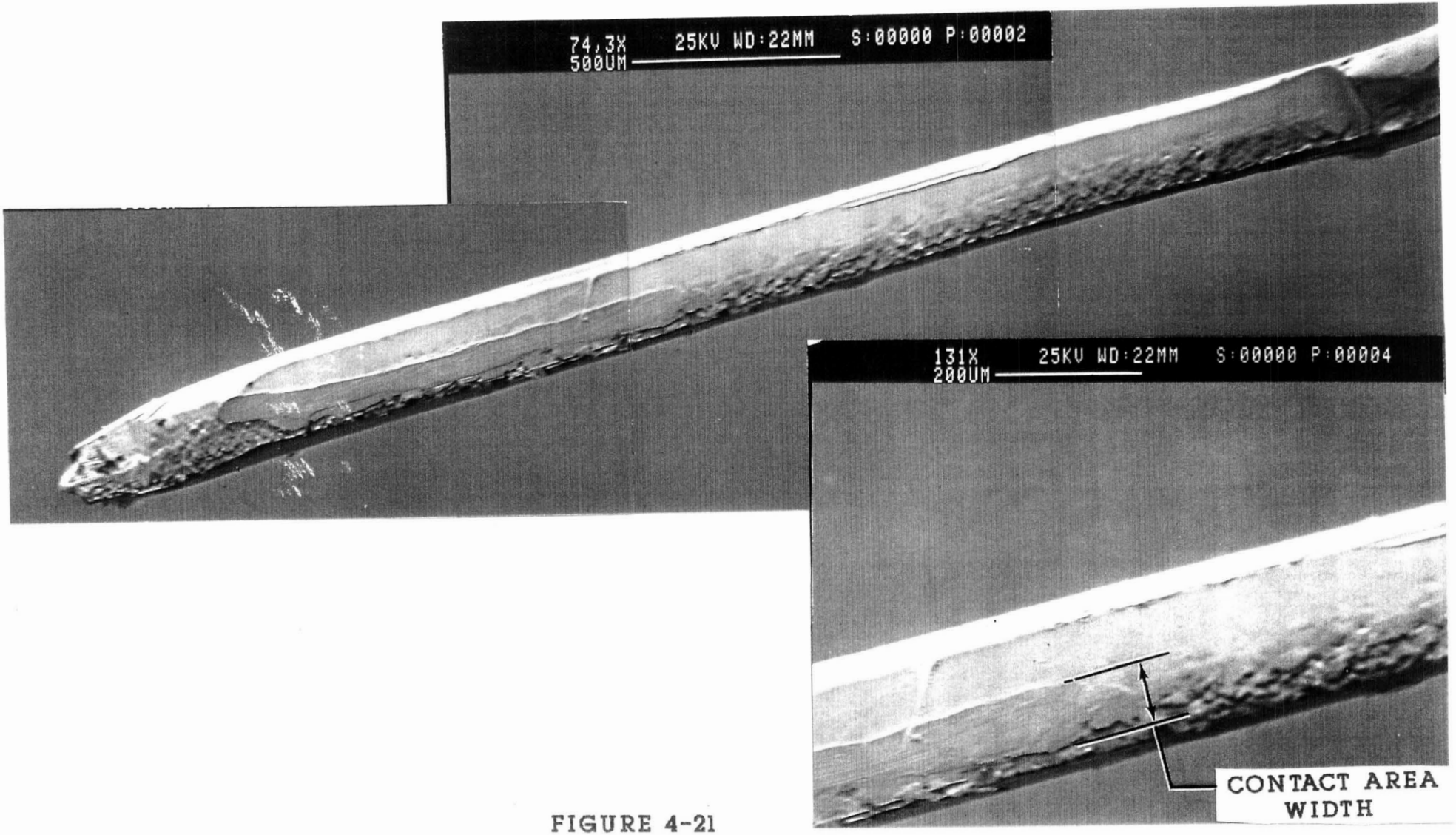


FIGURE 4-21

SEM- PHOTOMICROGRAPHS OF Ag PLATED PIN CONTACT AREA (ARROW) OF AN IC FROM BOARD NO. 1. THE SURFACE AREA APPEARS ROUGH OVER THE LOWER HALF OF THE FACE. THE WIDTH OF THE CONTACT AREA IS LESS THAN HALF OF THE PIN THICKNESS (LOWER VIEW).

FIGURE 4-22

SEM-PHOTOMICROGRAPH OF A Ag PLATED PIN OF IC SN7495N, 7349, BOARD NO. 1. THE DARK PITS (VOIDS) HAVE A HIGH Si CONTENT. THE 'ORANGE PEEL' OR 'MUD CRACKING' EFFECT VIEWED THROUGH THE THIN PLATING (LOWER VIEW) IS INDICATIVE OF CORROSION.

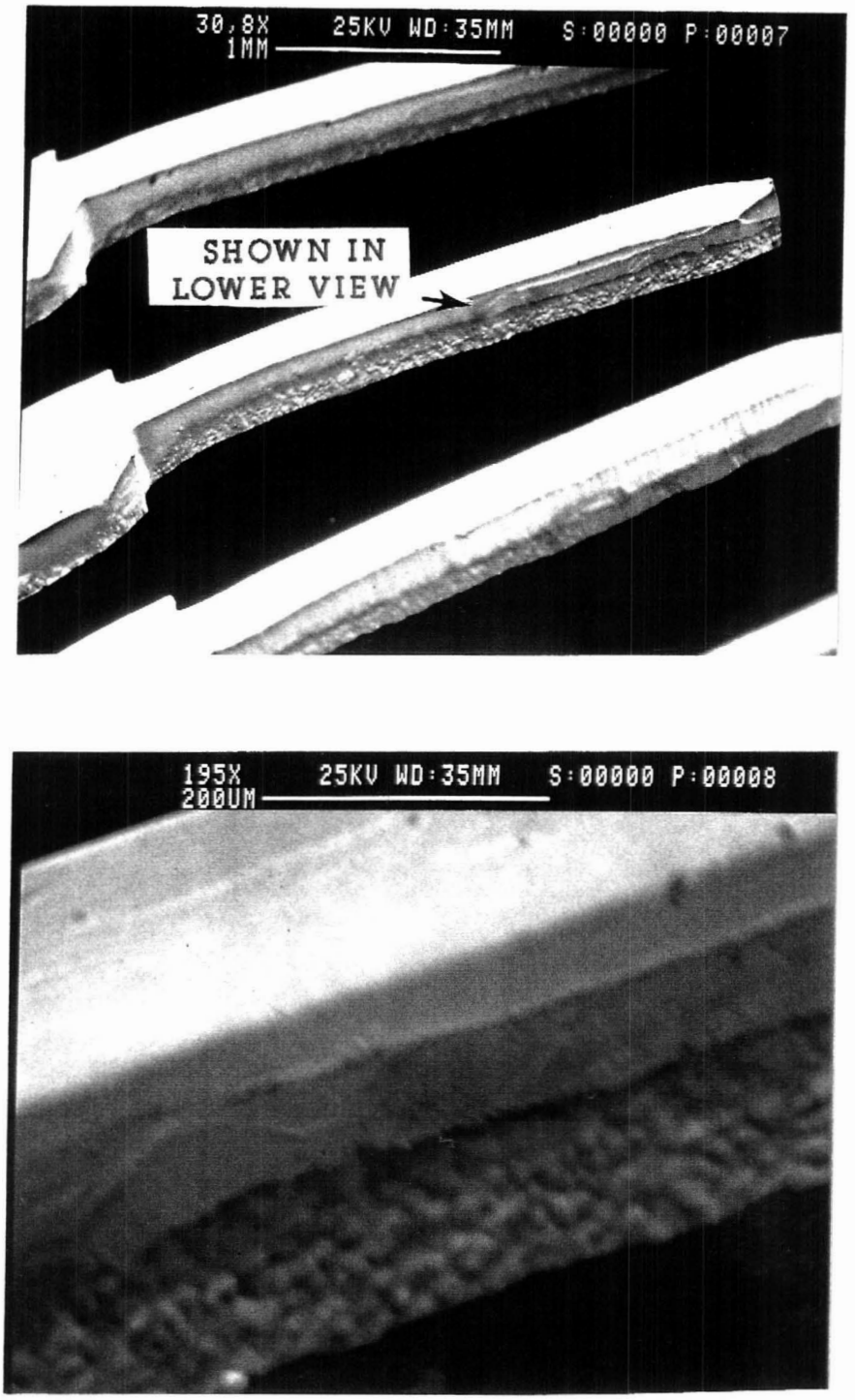


FIGURE 4-23

SEM-PHOTOMICROGRAPHS OF AN Ag PLATED PIN CONTACT AREA (ARROW) OF IC SN7495N, 7349, BOARD NO. 1. THE CONTACT AREA WIDTH IS SIGNIFICANTLY LESS THAN HALF OF THE PIN THICKNESS.

4.8.5 The IC's of this last model and manufacture date (SN7495AN, BS7349) were selected for the environmental test described in Section 5.3. This batch of IC's was selected for the apparent thin Ag plating and the anomalous, minimal contact areas of the pins which should produce a worst case environmental test conditon.

4.8.6 Other IC's such as the Z80's (Reference Section 4.5) have pin contact areas similar to the last IC pins analyzed (see Figure 4-23).

4.8.7 An IC with Sn plated pins was also found to have distinct variation in the surface profile across the contact area (see Figure 4-24).

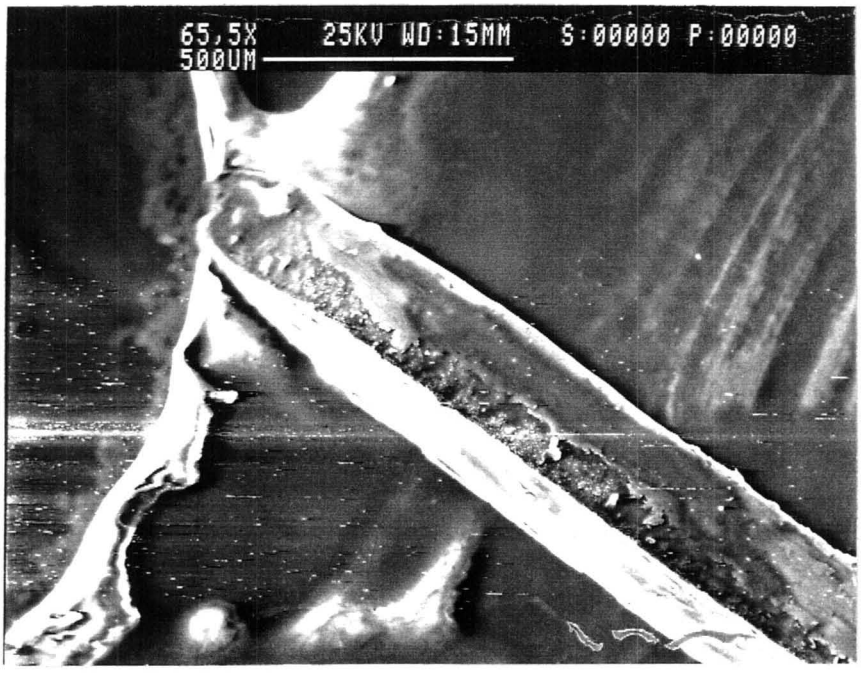


FIGURE 4-24

SEM-PHOTOMICROGRAPHS OF A Sn PLATED PIN CONTACT SURFACE OF IC SN74H04N, 7949, BOARD NO. 2. THE CONTACT EDGE SHOWS A DISTINCT VARIATION IN THE SURFACE PROFILE SIMILAR TO SOME OF THE Ag PLATED PINS.

4.9 SOCKETS

The socket contact area representative of the three boards were examined and analyzed by SEM/EDS and electron microprobe techniques.

4.9.1 The Board No. 1 socket contact area examined (see Figure 4-25) had a build-up of Ag over the Au plating. A flake of Ag_2S was found in the edge of the contact area. The EDS analysis indicated that the Au plating was undisturbed and free of porsity.

4.9.2 The Board No. 2 socket contact area examined (see Figure 4-26) had a build-up of Sn over the Au plating. The socket is Cu with Au plating over a Ni flashing. There was a significant indication of the Ni, but no Cu in the contact area, which indicates that the Au was smeared. The presence of Ag suggests that a Ag plated IC pin had once been inserted into the socket. A white material found in several locations at or near the contact area was high in oxides of Sn.

4.9.3 The Board No. 3 socket examined (see Figure 4-27) was found to be a two piece structure consisting of an outer body with an insert which had 4 contact fingers. The body was identified as a Cu-Zn alloy which was Au plated over a Ni flashing on the exterior surface. The insert was identified as primarily Cu with the Au plating on all surfaces.

4.9.4 The black body type sockets used on Boards No. 1 and No. 2 (see Figure 4-28) provide two contacts per pin. As the pins are inserted the relatively soft Ag or Sn plating of the pin is deposited on the contacts to provide a low resistance couple between the pin and the contacts.

4.9.5 The type of socket used on Board No. 3 provides a minimum of two and possibly four contacts per pin (see Figure 4-28). The insert within the socket has four contact fingers to make contact with the IC pin.

4.9.6 The design of black body type socket to pin contact allows for a crevice corrosion situation to occur above and below the contact point. The Board No. 3 socket appears to be less susceptible to this problem due to the sharp edge contact configuration and the crevice created on only one side. Other factors such as the contact force also contribute to contact integrity.

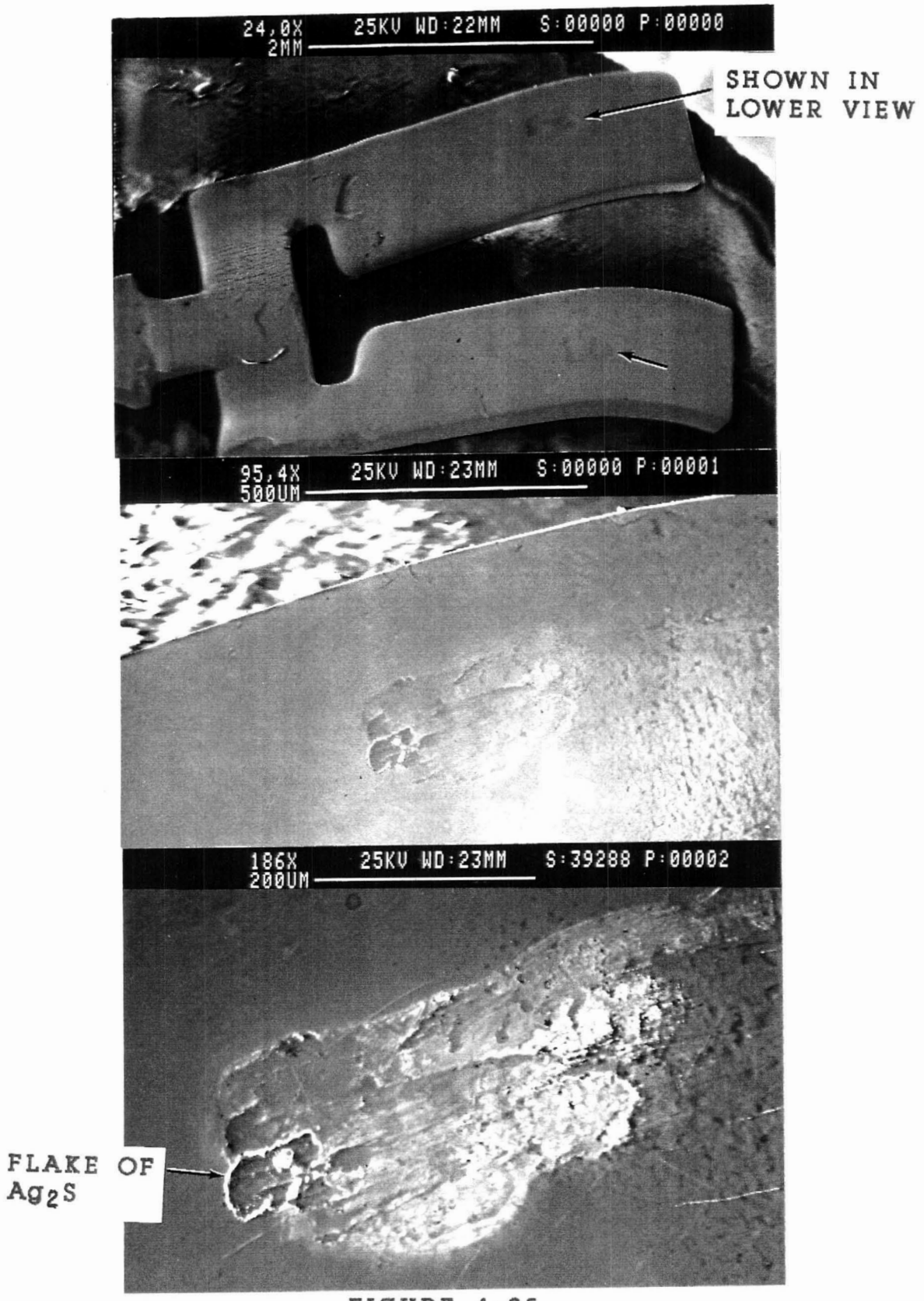


FIGURE 4-25

SEM-PHOTOMICROGRAPH OF AN OPENED SOCKET CLIP (TOP VIEW) FROM BOARD NO. 1. THE PIN CONTACT AREAS ARE IDENTIFIED (ARROWS). THE CONTACT AREA (LOWER VIEWS) IS PRIMARILY A DEPOSIT OF Ag, WITH SOME FLAKES OF Ag_2S.

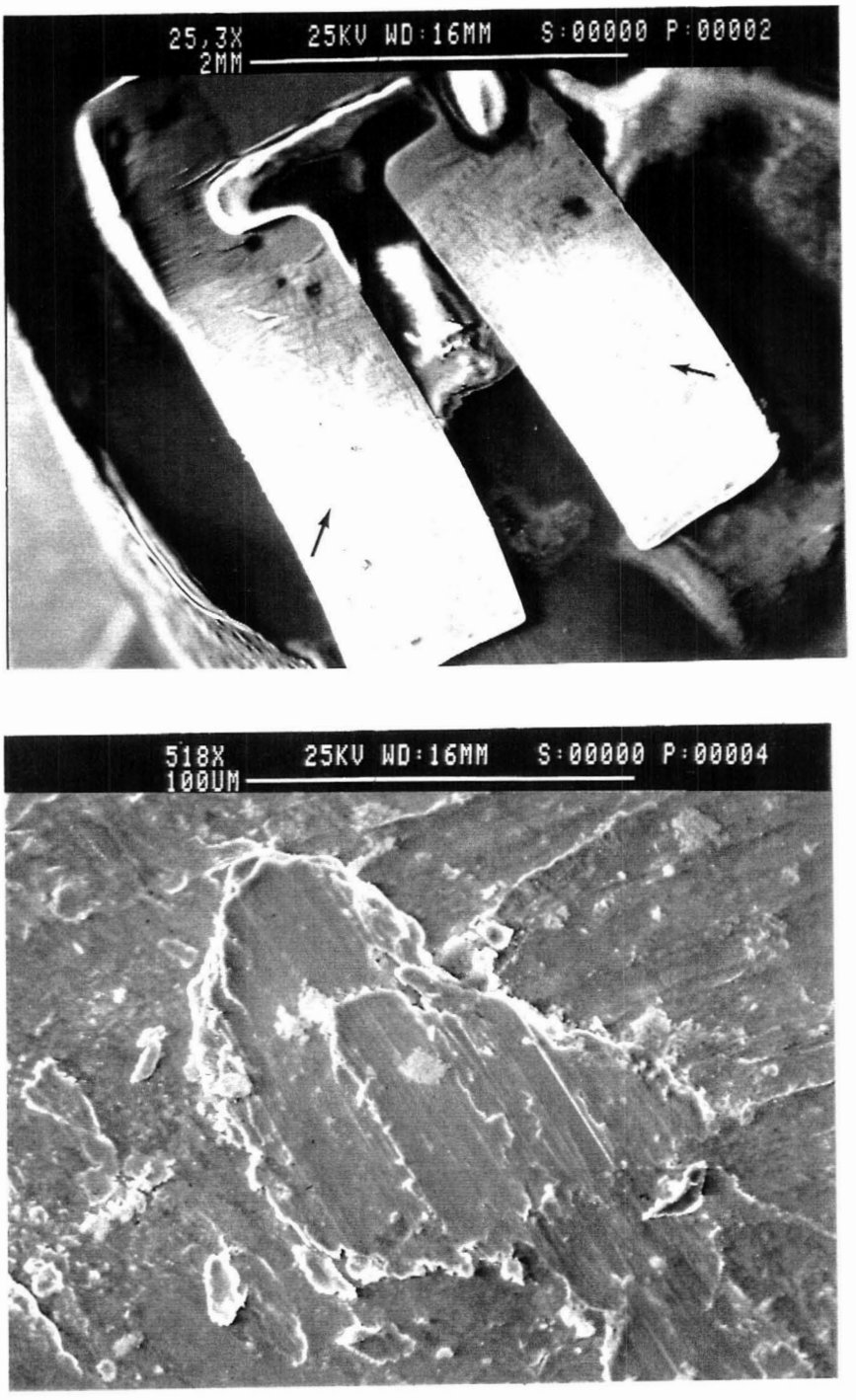


FIGURE 4-26

SEM-PHOTOMICROGRAPH OF AN OPENED SOCKET CLIP (TOP VIEW) FROM BOARD NO. 2. THE PIN CONTACT AREAS ARE IDENTIFIED (ARROWS). THE CONTACT AREA (LOWER VIEW) IS PRIMARILY A DEPOSIT OF Sn, WITH SOME PARTICLES OF SnO_2..

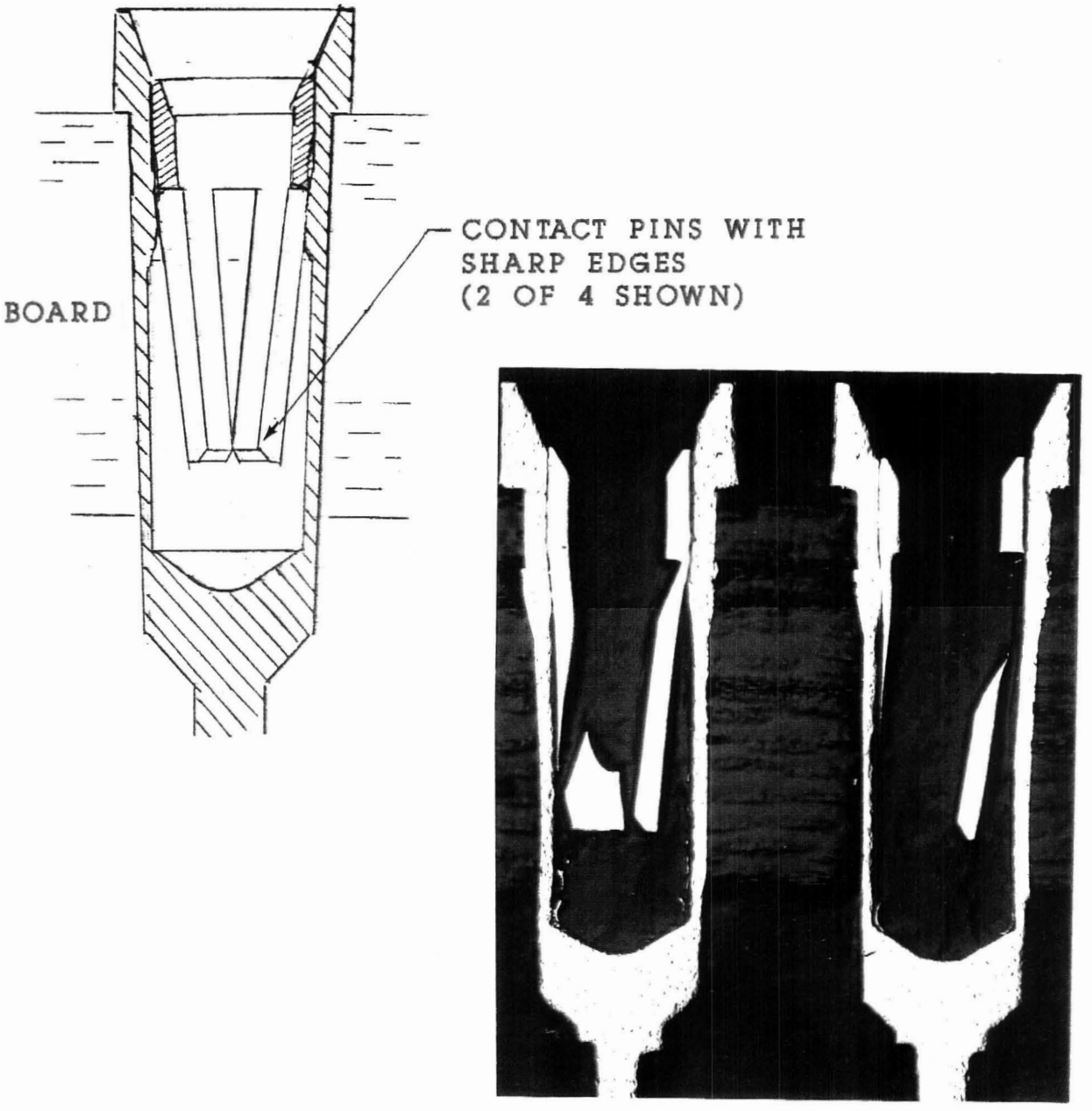
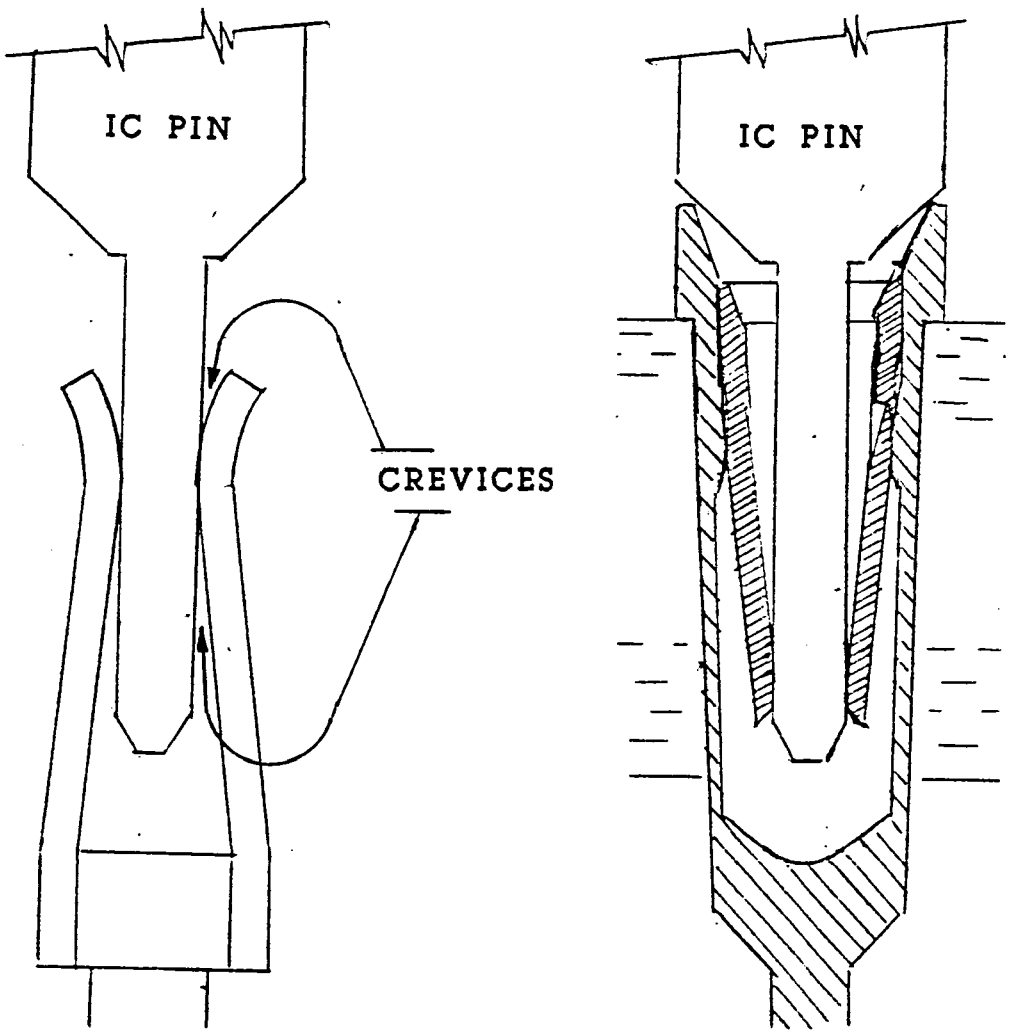


FIGURE 4-27

PHOTOMICROGRAPH (RIGHT) SHOWS CROSS-SECTION OF A SOCKET FROM BOARD NO. 3, AND A DRAWING (LEFT).



BLACK BODY TYPE

BOARD INSERT TYPE

FIGURE 4-28

THE PIN-SOCKET CONTACT OF THE TWO TYPES OF SOCKETS IS ILLUSTRATED.

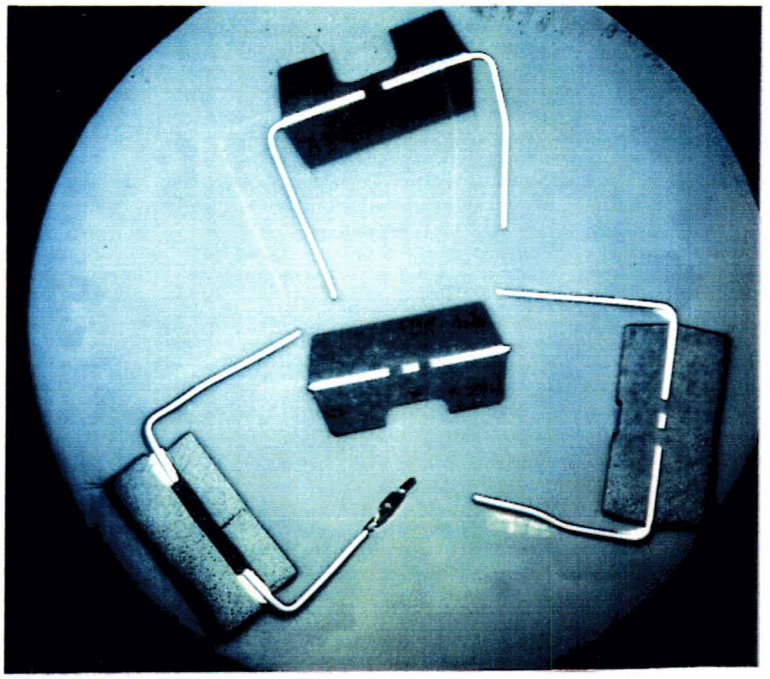
4.10 IC PACKAGES

Four IC's were metallographically mounted and sectioned to investigate the possibility of S migration along the pins into the package (see Figure 4-29).

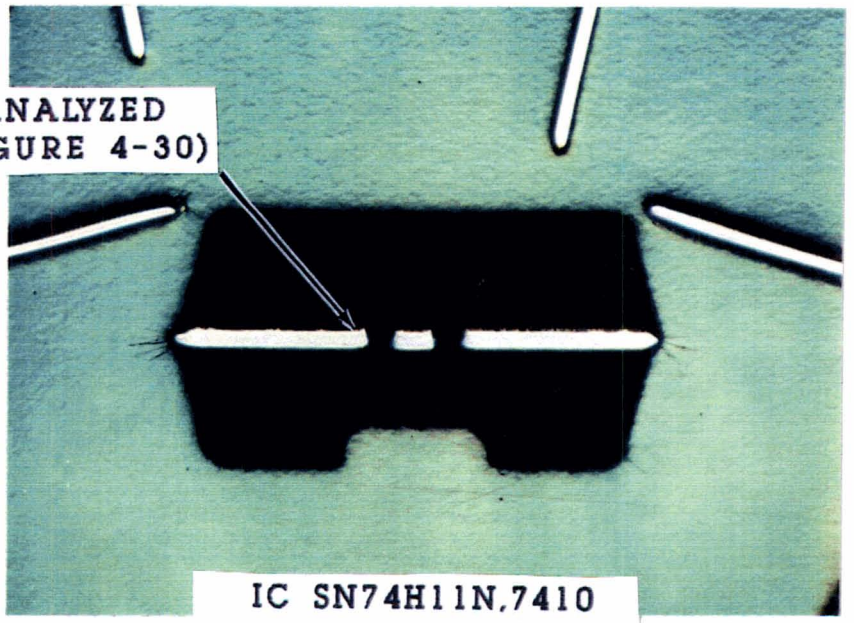
4.10.1 One IC pin package, SN74H51N, 7148, was analyzed for S content by EDXRF, SEM/EDS and electron microprobe/EDS. All three analytic methods indicated the package material contained S in trace quantities.

4.10.2 The four IC's were analyzed by microprobe/EDS for distribution of elements across the pin to body interface within the package for evidence of S along the interface (see Figure 4-30). No S was detected along the interface. The results of the elemental analysis are presented in Table 4-2.

4.10.3 Sulfur required in the minimum minor quantity of 1% to be detected by these techniques.



MAGNIFICATION: 4X



MAGNIFICATION: 10X

FIGURE 4-29

CROSS-SECTION OF THE FOUR IC's ARE SHOWN IN A METALLOGRAPHIC MOUNT (TOP). THE PINS WITH THE Ag_2S WERE REMOVED PRIOR TO MOUNTING TO PREVENT CONTAMINATION. AN EXAMPLE OF THE MICROPROBE ANALYSIS IS PRESENTED IN FIGURE 4-30. THE AREA ANALYZED IS IDENTIFIED ABOVE (ARROW).

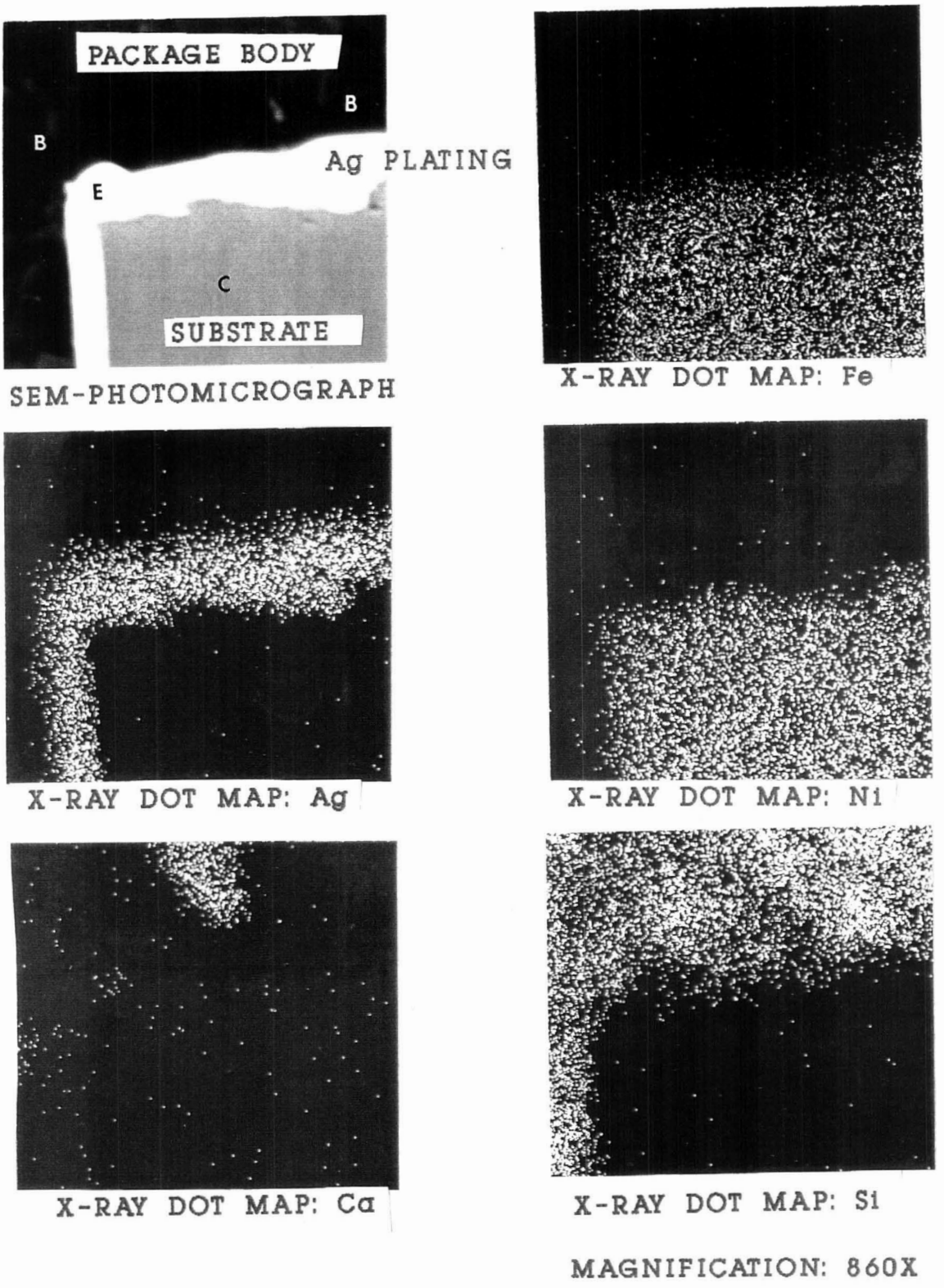


FIGURE 4-30

MICROPROBE ANALYSIS RESULTS OF IC SN74H11N ARE SHOWN. THE X-RAY DOT MAPS ARE OF THE AREA SHOWN IN THE SEM-PHOTOMICROGRAPH. NO SULFUR WAS DETECTED AT THE INTERFACE BETWEEN THE Ag PLATING AND THE PACKAGE BODY.

TABLE 4-2
MATERIAL ANALYSIS RESULTS OF IC PIN AND PACKAGE
ELECTRON MICROPROBE/SEM/EDS

IC		PIN		PIN TO BODY INTERFACE	BODY	
PART NUMBER	DATE CODE	BASE MATERIAL	PLATING MATERIAL		PACKAGE MATERIAL	BLOCK MATERIAL
SN74H11N	7410	Fe, Ni	Ag Minor (Si), (Fe)	----------	Si Minor (Al), Ca	N/A
SN74H04N	7949	Cu Minor Fe	Sn Minor (Cu), (Si)	----------	Si Minor (Al), (Sn)	N/A
DM74H00N	414	Fe, Ni	N/A	----------	Si Minor (Al)	N/A
1898-38-0		Fe	Sn	----------	Si Minor (Al)	Al

Note: The elements in brackets () maybe smeared from adjacent area or in the case of Al the polishing compound Al_2O_3.

5.0 TEST AND ANALYSIS

Electrical, mechanical, and environmental tests were performed on the LPS circuit board component parts.

5.1 INITIAL RESISTANCE MEASUREMENTS

All resistance measurements were made by 4-wire techniques utilizing a digital multimeter, Keithley Model 196.

5.1.1 Twenty IC's with heavily tarnished pins were selected on Board #1. The pin to post (pin contact) resistance was measured for each of the 14 pins of the 20 IC's. The range of contact resistance for each IC is presented in Table 5-1.

5.1.2 The total pin contact and wire wrap resistance of several IC pins were measured on each of the three boards. The wire-wrap wire insulation was stripped approximately 1 5/8 inches from the post and wrapped once around an adjacent post so that no stress would be expected upon the wire-wrap during the measurements.

5.1.2.1 First several heavily tarnished pins on Board No. 1 were selected. A blunt probe was used to make contact with the pins.

5.1.2.2 Then the same measurements were made with a sharp tipped probe to determine any differences in resistance due to the surface tarnish on the pins.

TABLE 5-1

RANGE OF CONTACT RESISTANCES
FOR TWENTY IC'S (BOARD NO. 1)
(IC PIN TO SOCKET POST)

NUMBER OF IC'S	RESISTANCE RANGE MILLIOHMS
1	7 - 8
5	12 - 14
2	12 - 15
2	12 - 16
3	13 - 14
6	13 - 15
1	13 - 16

5.1.2.3 Similar measurements were made on Boards No. 2 and 3 with a sharp tipped probe.

5.1.2.4 The results are presented in Table 5-2. The Board No. 1 contact resistance measurements made with the blunt probe were an average of 8.4 milliohms greater than when made with the pointed probe.

5.1.3 Wire leads were attached to IC pins on each board to measure only the contact resistance between the pin and post, excluding the probe contact resistance. The resistances: R_1, pin to post resistance; R_2, post to wire resistance; and R_t, pin to wire resistance were measured. The results are presented in Table 5-3.

5.1.4 New wire-wrap wires were installed on a socket from Board No. 1; this installation was designated test board ATB4. The wire to post resistance of all 14 wire-wraps were in the range of 24 to 26 milliohms stripped approximately 2-1/8 inches from the posts.

5.1.5 Due to the different lengths of wire-wrap wire used in the preceding measurements they can not be directly correlated. However, based on the resistance of 8.6 milliohms per inch of 30 gauge copper wire. The wire-wrap resistance can be equated. A comparison of the wire-wrap resistances is presented in Table 5-4.

TABLE 5-2

IC PIN TO WIRE-WRAP WIRE RESISTANCES

		RESISTANCE MILLIOHMS			
		BOARD NO. AND PROBE TYPE			
SET	LOC	1 (BLUNT)	1 (SHARP)	2 (SHARP)	3 (SHARP)
1	1	45	29	34	28
	2	36	27	29	35
	3	35	28	31	25
2	1	32	30	31	31
	2	35	26	29	34
	3	35	31	26	31
3	1	37	18	28	27
	2	23	18	28	27
	3	25	21	34	28
AVERAGE		33.7	25.3	30.7	29.4

TABLE 5-3

IC PIN TO WIRE-WRAP WIRE RESISTANCE

$R_1 + R_2 = R_t$

RESISTANCE MILLIOHMS

BOARD NO.	CHIP NO	R_1 PIN TO SOCKET POST	R_2 POST TO WIRE	R_t PIN TO WIRE
1	4	11.8	20.5	28.5
	5	10.6	24.3	33.5
2	4	8.5	21.5	26.8
	5	9.0	21.3	27.3
3	4	5.7	18.5	23.0
	5	5.5	18.8	23.7

TABLE 5-4

COMPARISON OF WIRE-WRAP

RESISTANCES - Rc

DESCRIPTION	M TEST MEASUREMENT (MILLIOHMS)	L INSULATION LENGTH (INCHES)	C_f CORRECTION FACTOR (L X 8.6) MILLIOHMS	Rc (MILLIOHMS)
NEW WIRE-WRAP ATB4	24-26	2 1/8	18.3	5.7-7.7
TABLE 5-3				
BOARD 1 - R_2	20.5-24.3	1 5/8	14.0	6.5-10.3
BOARD 2 - R_2	21.3-21.5	1 5/8	14.0	7.3-7.5
BOARD 3 - R_2	18.5-18.8	1 5/8	14.0	4.5-4.8

5.2 INITIAL ENVIRONMENTAL TEST

For this test, black body sockets from Board No. 1 were mounted on strips of perforated circuit board. Wire leads were soldered on pins of the 14-pin IC DIP's, and leads were wire wrapped on the mating socket posts. The test specimens were then placed in a humid H_2S rich environment.

5.2.1 The board designated ABT1 had an IC with Ag plated leads. Board ABT2 had Sn plated IC pins. Both boards used sockets with Au plated copper posts.

5.2.2 The boards were subjected to a humid H_2S environment for approximately 30 days. After the 30 days the conditions of the boards were documented. The H_2S was produced in a desiccator by adding H_2SO_4 to a Na_2S solution. The environment was regenerated on a weekly basis.

5.2.2.1 The Ag plated pins of the ABT1 IC were covered with a blackish-gray layer with some reddish-brown corrosion products showing through. The wire-wraps were covered with a gray coating, and some areas of the posts were also covered with a gray-green material (see Figure 5-2).

5.2.2.2 The Sn plated pins of the ABT2 IC were covered with reddish-brown corrosion products. The wire-wrap wires and posts appeared similar to those of ABT1 (see Figure 5-3).

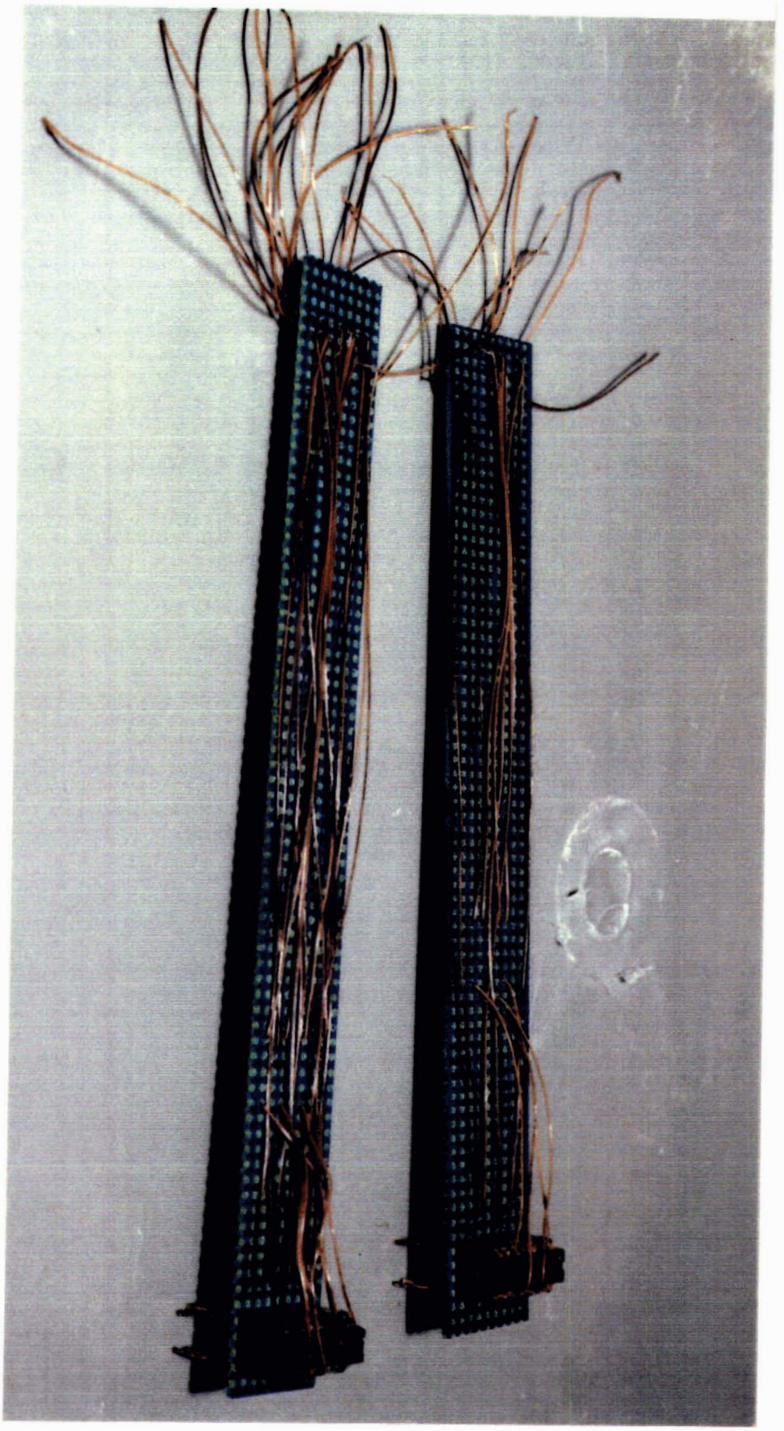


FIGURE 5-1

THE TWO TEST BOARDS, ABT1 AND ABT2, WHICH WERE SUBJECTED TO 30 DAYS OF A HUMID H_2S ENVIRONMENT ARE SHOWN.

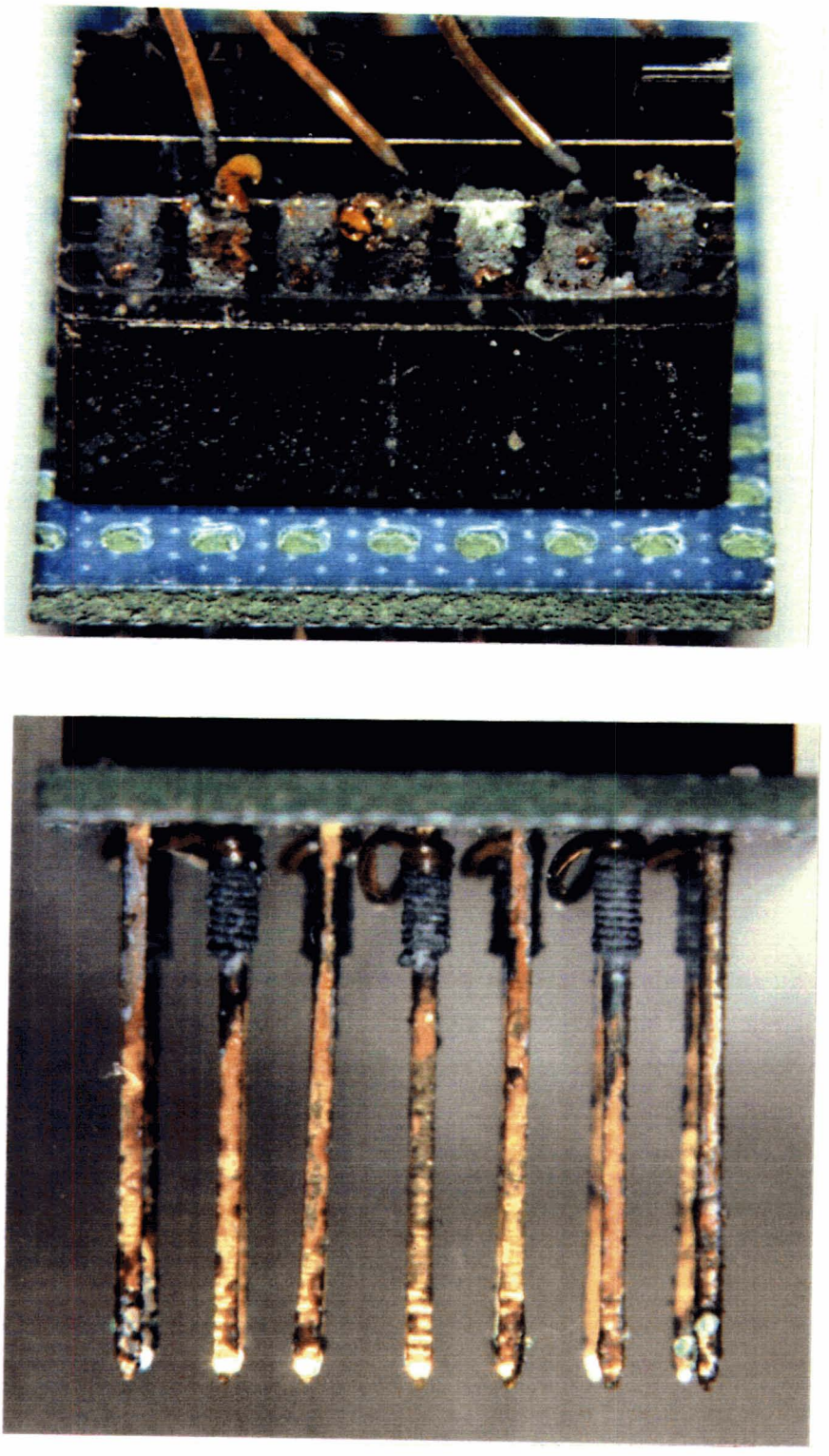


FIGURE 5-2

THE ABT1 IC AND SOCKET (TOP VIEW), AND THE SOCKET POSTS AND WIRE-WRAPS (LOWER VIEW) ARE SHOWN AFTER 30 DAYS EXPOSURE TO A HUMID H_2S ENVIRONMENT. THE IC PINS WERE COVERED WITH A BLACKISH-GRAY LAYER WITH SOME REDDISH-BROWN CORROSION PRODUCTS SHOWING THROUGH. THE WIRE-WRAPS WERE COVERED WITH A GRAY COATING, AND SOME AREAS OF THE POSTS WERE ALSO COVERED WITH A GRAY-GREEN MATERIAL.

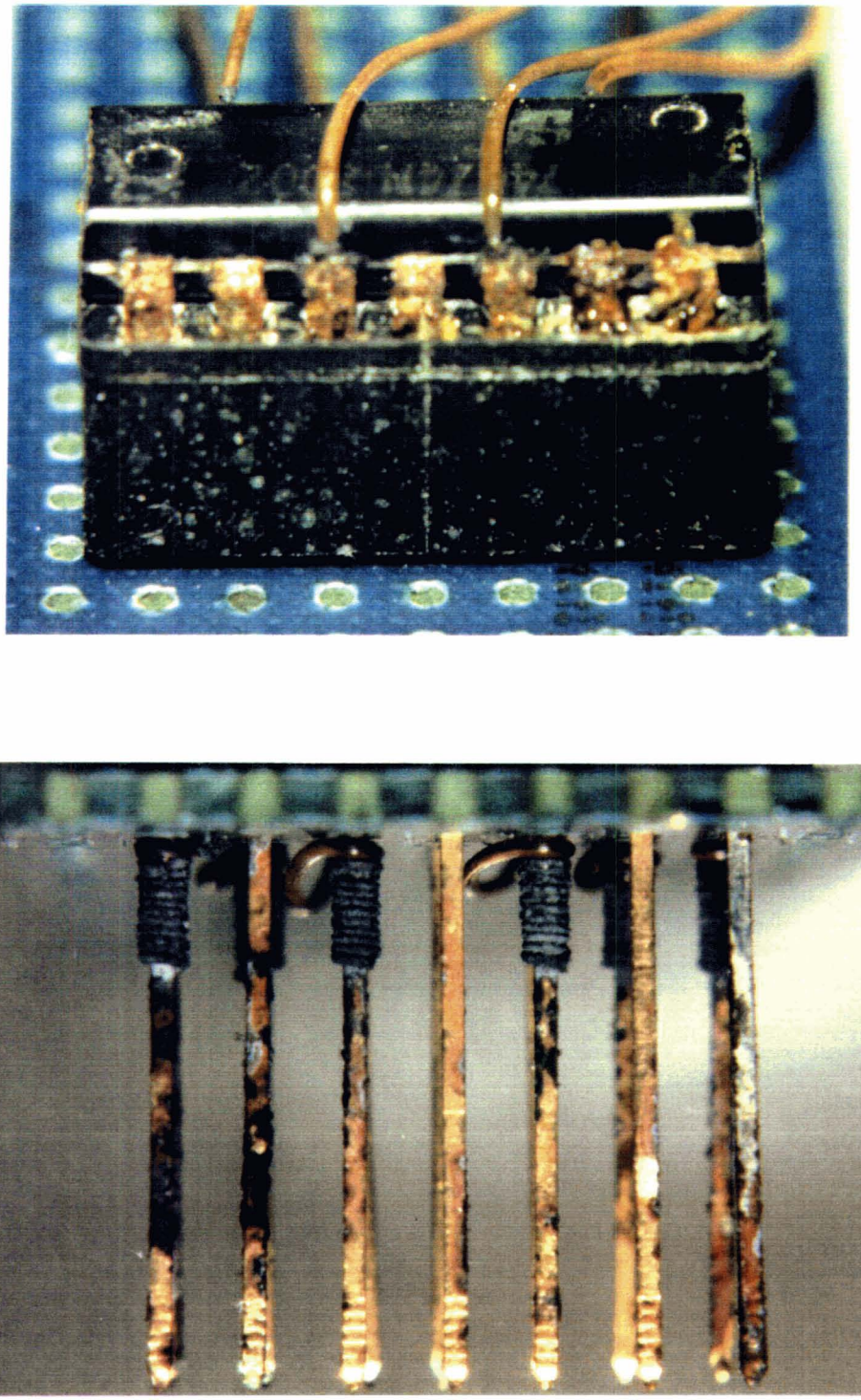


FIGURE 5-3

THE ABT2 IC AND SOCKET (TOP VIEW), AND THE SOCKET POSTS AND WIRE-WRAPS (LOWER VIEW) ARE SHOWN AFTER 30 DAYS EXPOSURE TO A HUMID H_2S ENVIRONMENT. THE IC PINS WERE COVERED WITH REDDISH-BROWN CORROSION PRODUCTS. THE WIRE-WRAPS WERE COVERED WITH A GRAY COATING, AND SOME AREAS OF THE POSTS WERE ALSO COVERED WITH A GRAY-GREEN MATERIAL.

5.2.2.3 The boards were allowed to dry out for over a week in the airconditioned laboratory environment before resistance measurements were made. Since no resistance measurements were made prior to the exposure, a baseline was selected on a wire resistance of 8.6 milliohms per inch of wire and a combined contact/wire-wrap resistance of 16 milliohms. The maximum, minimum, and average resistance increases for each board are presented in Table 5-5 and the resistance between adjacent socket posts for each board is presented in Table 5-6.

5.2.2.4 The circuit resistances were remeasured after 90 days. The resistance between adjacent posts had not changed significantly. However, the circuit resistances on test board ABT1 had increased significantly.

5.2.2.5 The circuit resistances of the test board ABT1 were measured again approximately 120 days after the environmental exposure.

TABLE 5-5
INCREASE IN CIRCUIT RESISTANCE

IDENTIFICATION	RESISTANCE (OHMS)		
TIME OF MEASUREMENT AFTER EXPOSURE	7 DAYS	90 DAYS	120 DAYS
TEST BOARD ABT1			
RESISTANCE INCREASES			
MAXIMUM	1.200	18.988	19.158
MINIMUM	0.065	0.316	0.314
AVERAGE	0.248	4.167	4.282
TEST BOARD ABT2			
RESISTANCE INCREASES			
MAXIMUM	0.026	0.108	N/A
MINIMUM	0.005	0.007	N/A
AVERAGE	0.017	0.040	N/A

TABLE 5-6

INSULATION RESISTANCE BETWEEN ADJACENT PINS

BOARD IDENTIFICATION	RESISTANCE OHMS	
	ABT1	ABT2
MAXIMUM RESISTANCE	267.0 M	> 300.0 M
MINIMUM RESISTANCE	116.0	11.0 K
AVERAGE RESISTANCE	24.0 M	198.0 M

5.3 CYCLIC/ENVIRONMENTAL TEST

This test consisted of cycling, installing and removing, 14-pin IC DIP's in sockets. The second step was to measure the contact resistance of pin to socket connection. The third step was to solder wire leads on 8 pins of the 14-pin IC DIP's, wire wrap leads on the mating socket posts, and then measure the individual circuit resistances. The test specimens were then placed in a H_2S rich environment.

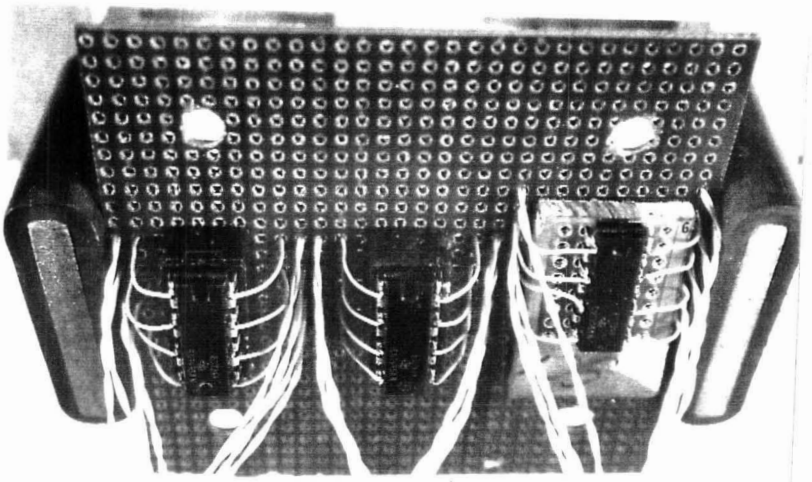
5.3.1 A socket was removed from each of the 3 boards, and a 14-pin IC dip was inserted and removed from the socket for a total of 100 cycles. An extractor and an installing tool were used for this operation. The contact resistances of each pin to socket connection were measured for the socket from each board. The high and low resistance readings for each socket are presented in Table 5-7.

5.3.2 The sockets were prepared for environmental test. The three sockets were mounted on a piece of perforated circuit board with 8 of the 14 pin contacts wired for testing. IC's, P/N SN7495AN with a date code of BS7349, were installed in each socket. These used IC's were selected for the minimal Ag plating on the pins. The test board ATB3 is shown in Figure 5-4.

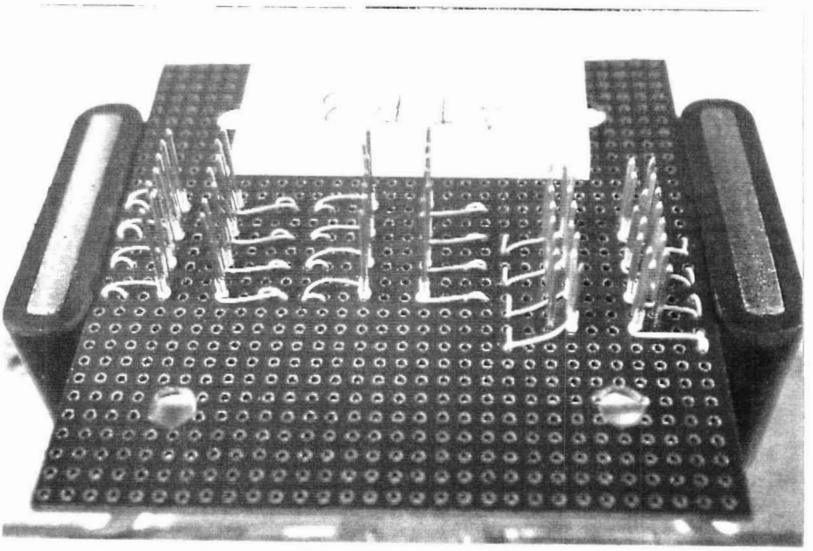
5.3.3 Circuit resistance measurements were made of all of the wired IC pin circuits. The test board was subjected to a humid H_2S/HCl

TABLE 5-7
PIN TO SOCKET CONTACT RESISTANCE
AFTER 100 14-PIN IC DIP INSTALLATION CYCLES

BOARD NO.	RESISTANCE - MILLIOHMS		
	HIGH	LOW	AVERAGE
1	14	11	12.2
2	15	12	13.1
3	13	11	12.1



IC/SOCKET SIDE OF TEST BOARD ATB3



WIRE-WRAP/SOCKET POST SIDE OF TEST BOARD ATB3

FIGURE 5-4

TEST BOARD ATB3 IS SHOWN PRIOR TO THE ENVIRONMENTAL EXPOSURE.

environment in the temperature range of 72° to 80°F. The H_2S/HCl environment was produced by adding a H_2SO_4/HCl solution to a Na_2S solution.

5.3.4 After 4 days in the H_2S/HCl environment the test board was removed from the environment, and allowed to dry for 2 days before circuit resistance measurements were made. The wire-wrap posts on the Board No. 2 socket were all discolored gray-green, and the exposed wire-wrap wires on all three board sockets were gray, and the silver plated pins were gray-black.

5.3.5 The test board, ATB3, was placed in a primarily H_2S environment for an additional 8 days. After which, the board was removed, allowed to dry, and the circuit resistance measured. A summary of the circuit resistance data is presented in Table 5-8.

5.3.6 The gold plated socket posts of boards No. 1 and 3 were still shiny. However, the exposed Ag plated wire-wrap wires and the board No. 2 posts were all gray in color (see Figure 5-5).

5.3.7 The circuit resistances were measured again approximately 60 days after the last exposure to the H_2S environment. The Boards No. 1 and No. 2 circuit resistances had increased while the Board No. 3 circuit resistances had remained relatively unchanged.

TABLE 5-8
CYCLIC/ENVIRONMENTAL TEST RESULTS
CIRCUIT RESISTANCE
(MILLIOHMS)

DAYS OF EXPOSURE	0	4	12	60 DAYS AFTER EXPOSURE
BOARD NO. 1				
MAXIMUM	221	272	816	1030
(INCREASE)		(51)	(595)	(809)
MINIMUM	206	217	250	250
(INCREASE)		(11)	(44)	(44)
AVERAGE	215	233	382	542
(INCREASE)		(18)	(167)	(327)
BOARD NO. 2				
MAXIMUM	244	304	2587	3954
(INCREASE)		(60)	)(2343	(3710)
MINIMUM	215	225	270	443
(INCREASE)		(10)	(55)	(228)
AVERAGE	228	246	905	1489
(INCREASE)		(18)	(677)	(1261)
BOARD NO. 3				
MAXIMUM	220	235	254	257
(INCREASE)		(15)	(34)	(37)
MINIMUM	202	211	226	225
(INCREASE)		(9)	(24)	(23)
AVERAGE	214	225	240	242
(INCREASE)		(11)	(26)	(28)

5.3.8 The high resistance circuits of Boards No. 1 and No. 2 were the results of pin to socket contact resistance. The wire-wrap post to wire-wrap resistances were in the range of 110 to 120 milliohms.

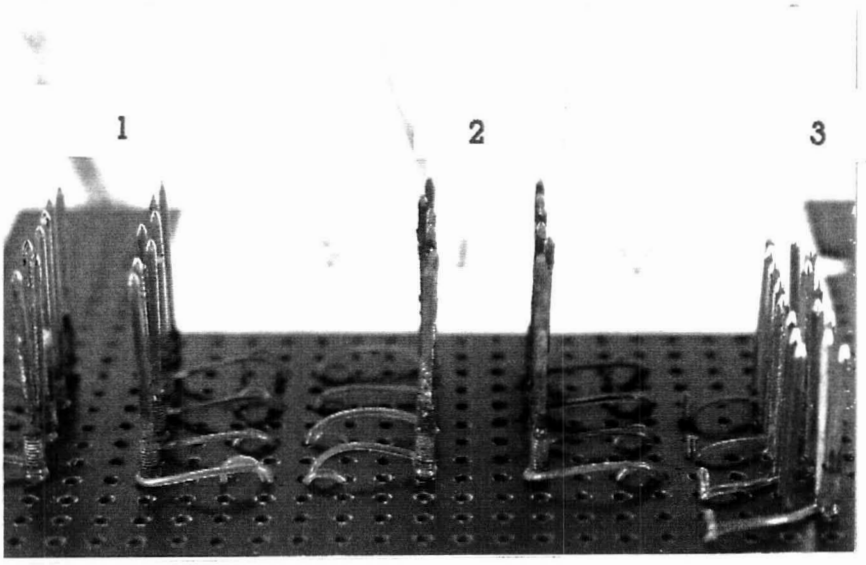


FIGURE 5-5

THE BOARD NO.2 SOCKET POSTS (CENTER) ARE CORRODED AFTER 12 DAYS OF ENVIRONMENTAL TESTING. TEH ADJACENT Au PLATED POSTS (BOARDS NO. 1 AND 3) ARE UNEFFECTED.

5.4 WIRE-WRAP ENVIRONMENTAL TEST

A section was cut from each of the three boards submitted for evaluation. The wire-wrap wire to wire-wrap post resistance of approximately 40 wire-wraps was measured on each board section. The sections were then subjected to 8 days of exposure to the H_2S environment. The post test and pretest wire-wrap resistances were virtually identical for all three board sections. In all cases the wire was severely tarnished and the posts on the Board No. 2 section were severely corroded, as previously illustrated in Figure 5-5. The resistances were remeasured after 60 days and found to still be unchanged.

5.5 ENVIRONMENTAL TEST OF "CONTACT RE-NU AND LUBE"

5.5.1 IC's with and without "Re-Nu and Lube" applied to the pins were subjected to an 8-day exposure to the H_2S environment. "Contact Re-Nu and Lube" P/N MS-238 is an aerosol spray product of Miller-Stephenson Co., Inc. It contains a hydrocarbon lubricant. "Re-Nu and Lube" was sprayed on the relatively clean pins of two IC's. A set of IC's was also tested without any coating applied.

5.5.2 When removed from the environment after 8 days of exposure the pins of both sets of IC's had turned black with Ag_2S formation.

5.6 WIRE FLEXURE TESTS

5.6.1 Wire-wrap wires from all three boards, as well as, reference wire from the Development

Testing Branch, DM-MED-2 supplies, and SPC stock were subjected to a 180° flexure test. The objective was to assess the work hardening or imbrittlement of the wire-wrap wires due to aging. The individual uninsulated sections of wire were clamped vertically in a fixture (see Figure 5-6). The wire was then bent 90° flat in one direction for half a cycle then straightened and bent flat in the opposite direction to complete the first cycle.

5.6.2 Three types of wire samples were tested:

5.6.2.1 Straight or relatively straight pieces from straight runs on the 3 boards, and straight reference specimens. The reference specimens were obtained from SPC stock and the DM-MED-2 supplies used to fabricate test board ATB4.

5.6.2.2 Wrapped wires from boards No. 1, 2, 3 and test board ATB4 were tested. First the individual wire-wrap posts were removed from the sockets. Then the individual wires were unwrapped from the posts and straightened. Two test specimens were obtained from each wire-wrap.

5.6.2.3 Wire-wrap specimens from the three board sections which were subjected to the H_2S environment (Reference Section 5.4) were also tested.

5.6.3 Twenty of each of the eleven types of wire test specimens were tested. The results are presented in Table 5-9.

5.6.3.1 The two types of reference wire should be relatively close. The 0.7 cycle difference between the DM-MED-2 wire (6.3 cycles) and the SPC stock wire (5.6 cycles) can be partially attributed to the fact that the SPC wire was received in a 3-inch diameter coil. The DM-MED-2 reference wire was in the form of short straight sections which were probably removed from a spool and cut and stripped for installation. The SPC stock wire was bent more prior to testing.

5.6.3.2 In the case of the straight Boards No. 1 and No. 3, the straight wire was restrained from vibrating freely. However, the Board No. 2 wire was hanging loose like spaghetti, so that it could vibrate in the cooling air stream. Therefore, the Board No. 2 wire was 1.6 cycles less than the other two boards.

5.6.3.3 The wire-wrap wire has a cyclic life that may correspond to its age and/or exposure life. The oldest board (No. 1) took the lowest number of cycles for failure, 2.3, while the new wire from test board ATB3 required 3.5 cycles.

TABLE 5-9

WIRE FLEXURE TEST

AVERAGE NUMBER OF CYCLES TO FAILURE

SOURCE OF WIRE	TYPE OF WIRE		
	STRAIGHT	WIRE-WRAP	H_2S EXPOSED WIRE-WRAP
BOARD NO. 1	4.9	2.3	1.8
BOARD NO. 2	3.3	2.9	2.8
BOARD NO. 3	5.2	3.3	3.4
REFERENCE DM-MED-2	6.3	3.5	---
SPC STOCK	5.6	---	---

5.6.3.4 There was no noticeable difference between the cyclic life of the original board wire-wraps and those exposed to H_2S, except for board No. 1. Board No. 1 had previously seen significant in-service exposure and the H_2S had already penetrated to the Cu of the wire-wrap wires prior to the H_2S exposure. So during the test the humid H_2S environment attacked the Cu directly, and significantly weakened the wire.

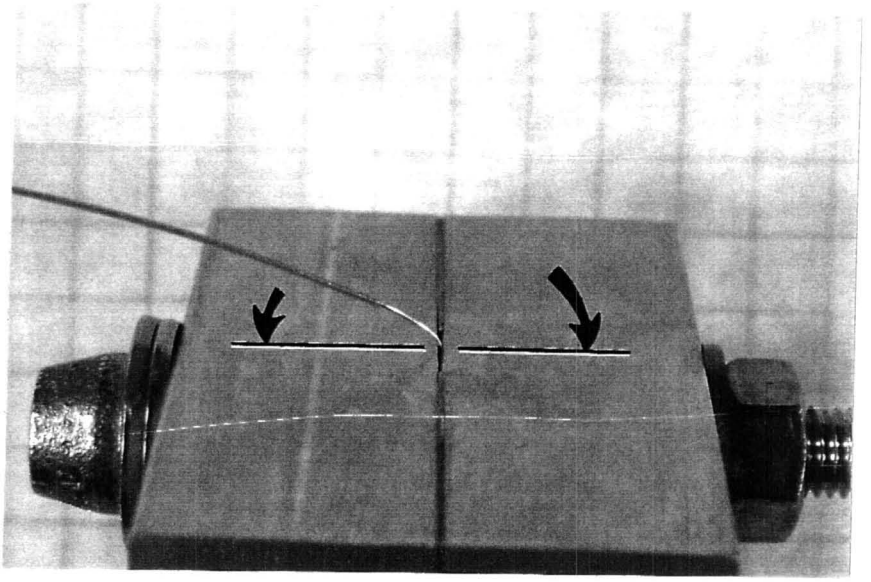


FIGURE 5-6

THE WIRE FLEXURE TEST FIXTURE IS SHOWN. THE 180° ARC OF BENDING IS ILLUSTRATED.

5.7 IC FUNCTIONAL TEST

The IC's removed from LPS circuit boards during troubleshooting procedures (Reference Section 4.6) were sent to the Texas Instrument (TI) facilities in Sherman, Texas for functional testing. The IC pins were cleaned prior to being tested.

5.7.1 Of the two 4 x 4 register files, Model SN74170N, removed from the same board, the one with the date code of 7627 failed several of the functioanl test sequences. Anomalous conditions were recorded on all four output pins (6, 7, 9, and 10). The high level output current (I_{oh}) exceeded the maximum limit of 30 microamps on pins 6, 7, and 9. In addition, the low level output voltage (V_{ol}) exceeded the maximum limit of 0.4 volts on pins 9 and 10. The TI RQA personnel indicate that this IC would definitely cause an anomalous circuit board condition.

5.7.2 Of the two IC's, SN74LS170N and SN74181N, removed from the second circuit board the 4 x 4 register file with open collector outputs, SN74LS170, 8044, failed several test sequences. Pin 12 the write-enable input (Gw) exceeded the maximum current limit of 0.2 milliamps at an input voltage of 7 volts. The TI RQA personnel indicated that this anomaly would probably not cause a circuit board failure. A review of the work order submitted with the IC's indicates that the subject IC's were isolated as the

probable cause of the board failure using cold spray. The circuit board failure was not verified or isolated during ambient testing.

5.7.3 The IC pin tarnish didn't create a contact resistance problem.

5.7.4 These specific circuit board failures were apparently not due to tarnishing of the Ag plated pins.

5.8 CONTACT RESISTANCE CIRCUIT TEST

With a steady state DC voltage on an IC circuit the contact resistances in the range of one ohm would drop the device input voltage only 2% with a device input impededance of 50 ohms if the input impedance were in the thousand ohm range the voltage drop becomes insignificant. It was, therefore, decided to look at the effect of the contact resistances on a high frequency 20 megahertz signal.

5.8.1 Initially a test of the test board ABT1 contact circuit which had increased by 1.2 ohms was tested. The circuit consisted of a twisted pair of 30 gauge wires, 10 inches long; one wire-wrapped to the post; and the other soldered to the mating pin. The circuit was in series between the signal generator and a 47 ohm load. The results were not consistent with the previous DC resistance measurements.

5.8.2 The DC circuit resistance was remeasured. The original circuit resistance shortly after

the environmental exposure was approximately 1.4 ohms. When remeasured the resistance was found to be 18 to 19 ohms.

5.8.3 As a result of this revelation all of the test circuit resistances were retested several months after the environmental exposures (Reference Sections 5.2.2.4, 5.2.2.5, 5.3.7, and 5.4).

5.8.4 The inductance of several test and reference circuits were measured with a Hewlett Packard Model 4192A LF Impedance Analyzer. The inductance of the 10 to 15-inch twisted wire pair test circuits were all approximately 0.3 microhenrys.

5.8.5 Several circuits were retested at 20 megahertz utilizing a Hewlett Packard Model 8082A Pulse Generator and a Tektronix Model 7854 Oscilloscope. All of the signal attenuation through the test circuits could be attributed to the expected circuit impedance, resistances and inductances, at 20 megahertz.

6.0 DISCUSSION

6.1 Silver was probably initially selected for coating IC pins because of its low electrical resistivity. The resistivity of Ag is 1.59 microhm-cm., while the resistivity of Cu, Au, and Sn are 1.72, 2.44, and 11.5 microhm-cm. respectively (11). The Ag plated pins should, therefore, have the lowest contact resistance of the available materials.

6.2 At atomospheric conditions where materials such as Cu will oxidize, Ag will only tarnish from exposure to atmospheric sulfides. The resistivity of the tarnish (Ag_2S) layers are reported to be significantly less than that of an equal layer of pure CuO (10). In many applications Ag may be highly desirable.

6.3 Based on the inspections, analysis (Section 4.0), and testing (subsections 5.1 and 5.7) conducted in this evaluation, there are no indications that the silver tarnish of the IC pins has been detrimental to the operation of the LPS. Earlier literature concerning the problem described the silver tarnish to only be a cosmetic problem (4).

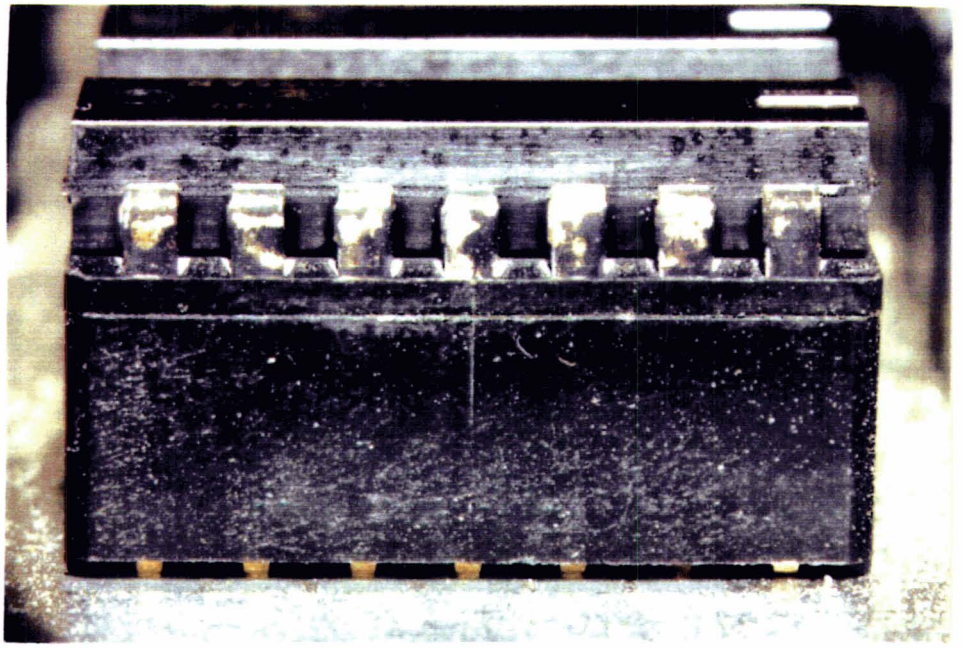
6.4 The worst application for Ag would probably be normally-open switch or relay contacts, which are exposed to a sulfide rich industrial or swamp type environment. The Ag plated contact faces would be continually exposed to the sulfides in the atmosphere, and become tarnished. In low current/voltage applications the Ag_2S on the contact faces would rapidly cause problems. However, in the case of the Ag coated IC pins, when they are inserted into a socket the Ag plating smears and deposits material on the mating contacts. This transfer process virtually builds up a puddle deposit of Ag so that more than a mere point contact exists between the pin and socket. It would probably require long/heavy exposures to a sulfide-rich environment alone to cause significant IC pin contact resistance problems.

6.5 From the environmental tests, contact resistances as high as 19 ohms were obtained with the Ag plated IC pins. These conditions were not necessarily the result of Ag tarnish, but from a combination of the high humidity, poor quality Ag plating, and the corrosiveness of the pin substrate material. Figure 6-1 illustrates the gross difference between a heavily tarnished IC from Board No. 1 and a corroded test specimen.

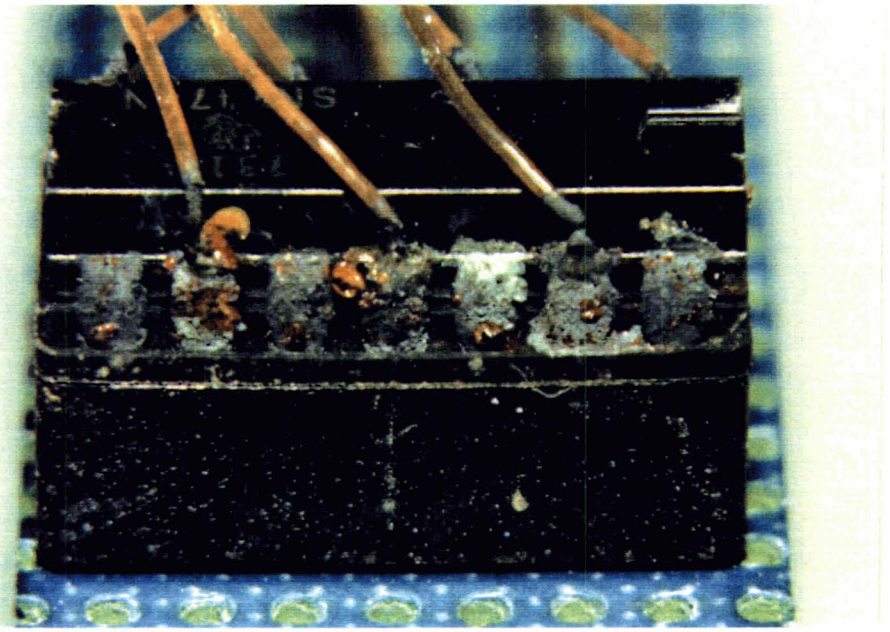
6.6 The test results emphasize the need for environmental controls in the LPS area. In addition to controlling the sulfides entering the LPS areas, humidity, temperature, and other contaminents should be controlled.

6.7 The environmental tests should be viewed as a worst case scenario, in which the LPS hardware is subjected to the humid subtropical swamp environment of KSC. The test results show that the moisture can be retained in the contact area and/or the corrosion process can continue until the deposit is fully dry.

6.8 Based on the condition of Board No. 1 and reports documenting problems encountered during the start-up phase of LPS it can be concluded that the LPS was not maintained in a proper environment (4, M2). The prevalance of stress corrosion cracking of the IC pins and dendritic growth on the pins indicates that some of the LPS hardware was maintained in a corrosive environment. However, since these first problems it appears that the LPS has been maintained in a proper environment, except for the presence of some atmospheric sulfides.



IC WITH TARNISHED PINS INSTALLED ON 12 YEAR OLD BOARD NO. 1 AS RECEIVED BY THE MTB.



IC WITH CORRODED PINS ON TEST BOARD ABT1 AFTER ENVIRONMENTAL TEST.

FIGURE 6-1

THE DIFFERENCE BETWEEN HEAVILY TARNISHED IC PINS (TOP) AND THE CORRODED TEST SPECIMEN WHICH PRODUCED CONTACT RESISTANCES AS HIGH AS 19 OHMS (BOTTOM) IS ILLUSTRATED.

7.0 RESPONSE TO QUESTIONS

7.1 WHAT IS THE SOURCE OF THE SILVER TARNISH CONDITION?

The silver tarnish is silver sulfide (Ag_2S) film, which is caused by the presence of sulfur compounds in the atmosphere. Some of the potential sources of atmospheric sulfur compounds, such as H_2S, in the KSC environment are listed below:

7.1.1 Swamp gases generated by the decomposition of vegetation.

7.1.2 Emmissions from the local coal fired electric power plants.

7.1.3 Emissions from some internal combustion engines.

7.1.4 Offgassing from some polymeric materials such as plastic panels, rubber gaskets and seals, and furniture.

7.1.5 Intestinal gases of animals.

7.2 DOES THE TARNISH EFFECT THE IC DIP'S INTERNALLY?

7.2.1 In the case of the IC's with the Ag plated leads, the Ag acts as a collector for the H_2S and therefore it probably doesn't cause any problem.

7.2.2 The IC's with Sn plated leads would be more likely to encounter a problem from the H_2S if any problem exists. Some work has been performed in this evaluation looking at the

IC leads within the cases with the SEM/EDS and electron microprobe; however, it will require an XPS with an ion gun attachment to perform the surface analysis required to answer this question.

7.2.3 Metal migration both within and on external surfaces of IC's has been documented; however, a phenomenon such as S migration has not been reported. This may be because traditional failure analysis techniques use materials such as H_2SO_4 to decapsulate the IC's.

7.3 WHAT IS THE EFFECT OF THE TARNISH ON IC SOCKETS AND OTHER COMPONENTS ON THE BOARD?

7.3.1 The primary area of concern is the effect of sulfides on the wire-wrap wires. In the process of forming the wire-wraps the exposed wires will receive some mechanical damage to the protective Ag coating. Over the long-term, sulfides and oxides will attack the copper beneath the Ag coating through the damaged areas (3).

7.3.2 The tarnish on the IC pins will have little effect on the contact resistance between the pin and socket. However, it will have a cosmetic effect if one insists on having shiny IC pins (4). Tarnish could be a significant problem with Ag plated switch contacts which are normally in the open circuit position. The exposed contact surfaces could become tarnished and increase the contact resistance.

7.3.4 The Au plated sockets appear to be uneffected by the environmental sulfides.

7.3.5 The unplated wire-wrap posts on Board No. 2 appear to be the second greatest area of concern. In a corrosive environment these unprotected Cu-Ni alloy posts pose a potential problem.

7.4 DOES THE WIRE-WRAP WIRE SHOW SIGNS OF DETERIORATION OR BRITTLENESS?

7.4.1 Metallographic examination of the tarnished wire-wrap wires on the worst case board, No. 1, indicate that significant corrosive attack had occurred only at the end of the wires.

7.4.2 The flexure tests indicate that the wire-wrap of the thin wires on the oldest board, Board No. 1, were probably the most embrittled/work hardened, and they also deteriorated the most during the environmental exposure.

7.5 WHAT ARE THE NEAR AND LONG TERM EFFECTS ON LPS HARDWARE MTBF?

7.5.1 The tarnish on the Ag plated IC pins should have no effect on the operation of an IC. However, the tarnish/deterioration of thin Ag coating on the wire-wrap wire does expose the copper wire to corrosive attack and could reduce the MTBF.

7.5.2 Gross failures of the air-conditioning system which maintains the LPS in a cool low humidity environment could be a significant factor in increasing the failure rate, lowering the MTBF.

7.5.2.1 The wire-wrap wires on the older boards are a primary concern in the event of air-conditioning failures. A warm humid environment could result in eventual mechanical failure of wire-wraps.

7.5.2.2 The susceptability of the Ag plated Fe alloy IC pins to stress corrosion is a potential problem in a warm moist environment.

7.5.2.3 The unplated Cu/Ni alloy of the socket posts on Board No. 2 are more susceptable to corrosion than the Au plated Cu sockets of the other boards.

7.6 EVALUATE PROTECTIVE COATINGS SUCH AS "CONTACT RE-NU AND LUBE"

7.6.1 In the test performed, the product "Contact Re-Nu and Lube" did not appear to provide any protection from the H_2S environment.

7.6.2 The Naval Research Laboratory has conducted a study of commercial organic coatings for protection of Au/Ag/Cu connectors in a H_2S environment (15). The following materials: Mil-C-81309, and Nye Tack Fluids 515 and 518, were found to provide the best protection of the 13 products evaluated. In this evaluation some of the products were found to be less effective than no coating at all.

7.6.3 It is not recommended to use a sticky oily corrosion inhibitor on the IC's, boards, or wire-wraps because it will collect environmental debris and possibly create other problems.

7.7 IS THERE A SUITABLE METHOD FOR CLEANING THE IC PINS, WIRE-WRAPS, SOCKETS, AND OTHER COMPONENTS?

7.7.1 An electrolytic method is often used to clean silver. However, the electrolytic method requires a solution of Na_2CO_3 or $NaHCO_3$, and NaCl. The electrolytic method is <u>not</u> recommended for the Ag plated IC's because of the steel substrate coupled with the often thin and porous Ag coating. The electrolytic solution can cause additional corrosion problems with the steel substrates which appear to be susceptable to stress corrosion cracking. None of the commercially available chemical cleaning agents are recommended for the same reason.

7.7.2 If it is deemed necessary to clean the IC pins, it is suggested that a mechanical method be used. It is suggested that an abrasive, such as Al_2O_3 with isopropyl alcohol (IPA) on a swab be used for removing the tarnish from the pins.

7.7.3 In the case of the wire-wraps nothing more than an IPA rinse is suggested. Attempting to clean the sockets is not recommended.

8.0 CONCLUSIONS

8.1 Although the silver tarnish, Ag_2S, on the IC pins is unsightly, the Ag_2S by itself is unlikely to be detrimental to the operation of the LPS.

8.2 The environmental tests, which eventually produced contact resistances as high as 19 ohms, should be considered a worst case scenario. These tests emphasize the need for environmental controls to extend the longevity of the LPS. The tests, also, point out the deficiencies of the Ag plated IC pins.

8.3 It is the responsibility of the cognizant design and operating organization to perform analysis of the LPS circuits to determine the impact of contact resistances as great as 19 ohms upon the system operations.

9.0 RECOMMENDATIONS

If maintained in a proper environment the LPS hardware could be expected to have a significantly extended operational life. There are three areas which should be stressed in the future:

a. Operations and Maintenance
b. Maximizing MTBF
c. Materials Selected for Future LPS Hardware

9.1 OPERATIONS AND MAINTENANCE

9.1.1 The airconditioning system for the LPS equipment should maintain the temperature at 70°F $\pm$ 5°F with a relative humidity of 45% $\pm$ 5%.

9.1.2 The simpliest method of minimizing the sulfides in the LPS environment is to install charcoal filters in the airconditioning system (M1). The filters should be replaced periodically.

9.1.3 Keep the LPS hardware free of environmental debris, dust, and dirt and other contaminants by particulate filtration.

9.2 MAXIMIZING THE MTBF

9.2.1 To maximize the MTBF it is suggested that 100% screening of replacement IC's be performed prior to installation in the individual circuit boards (13). This screening should include:

a. Particle Impact Noise Detector (PIND) where applicable
b. Burn-in (168 hours at 125°C)
c. Final electrical test (-55°C, +25°C, and +125°C)

9.2.2 Maintain an active preventive maintenance program of the airconditioning systems and other systems which support the LPS such as the Uninterruptable Power System (UPS).

9.2.3 To prevent any further deterioration of the wire-wrap wires the following steps may be considered. Clean the wire-wrap side of the boards with a solvent rinse, dry the boards, and apply a conformal coating to the wire-wraps.

9.3 MATERIAL SELECTIONS FOR FUTURE LPS HARDWARE

9.3.1 The continued use of plug-in IC sockets instead of soldered IC connections is advisable for the sake of maintenance. The unsoldering of failed IC's and resoldering of new IC's result in damage to a significant number of circuit boards which are scrapped (13).

9.3.2 Based on this evaluation the following materials should be required:

9.3.2.1 Sockets with wire-wrap posts of Cu alloys appear desirable with a mandatory Au plating with Ni flashing on all surfaces.

9.3.2.2 Wire-wrap wire of Cu wire is desirable with a Au coating instead of Ag. The Au requires a Ni flashing on the Cu wire.

9.3.2.3 IC pins of Cu or Fe based alloys appear satisfactory with Sn plating. Poor quality platings and corrosive environments may cause problems no matter what the materials are.

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16. Abstract

The Materials Testing Branch was requested to evaluate the effects of silver "tarnishing" of components of the Launch Processing System. The area of most significant concern found is the "tarnish" effects on the wire-wrap wires of the older LPS circuit boards. If maintained in the proper environment, the LPS hardware could be expected to have a significantly extended operational life, despite the relatively poor quality of some hardware.

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